4. Electronic Devices and Storage

4.1 2 200 V SiC MOSFET for Compact and Energy-Efficient Power Conversion Units

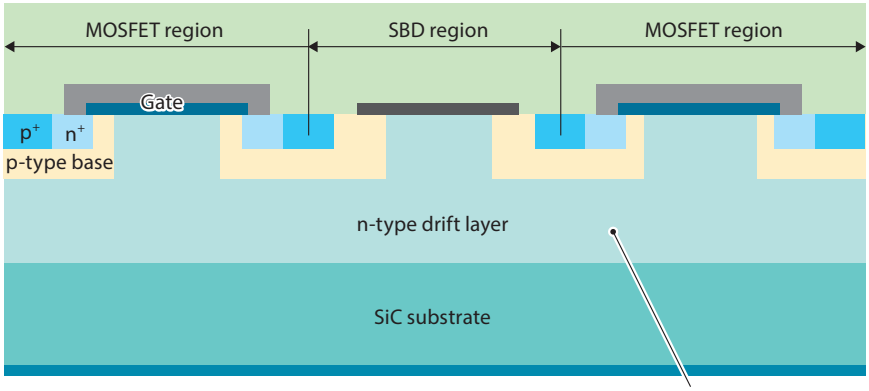
Toshiba Electronic Devices & Storage Corporation has developed a 2 200 V-class silicon carbide (SiC) power module which helps to reduce the size and energy consumption of power conversion units for photovoltaic (PV) power generation.

In recent years, increasing the input voltage of power modules for PV power generation applications to 1 500 V has been taken into consideration. Conventionally, three-level inverter circuits composed of silicon (Si) insulated-gate bipolar transistors (IGBTs) have been used for PV power generation applications. However, switching devices with higher blocking voltage and lower energy loss than those of Si IGBTs would help to achieve a two-level inverter circuit and thus make it possible to reduce the size and energy consumption of power conversion units.

We have developed a 2 200 V-class SiC metal-oxide-semiconductor field-effect transistor (MOSFET) based on our 1 700 V-class third-generation SiC power MOSFET. Device degradation of SiC MOSFETs in reverse conduction mode poses a reliability issue. To suppress device degradation, we adopted a structure with a built-in Schottky barrier diode (SBD). In addition, we optimized the drift layer design to increase blocking voltage without compromising a trade-off between on-resistance and blocking voltage.

Accelerated testing confirmed that the new SiC MOSFET provides improved neutron beam tolerance, which is required to ensure the long-term reliability of power conversion units.

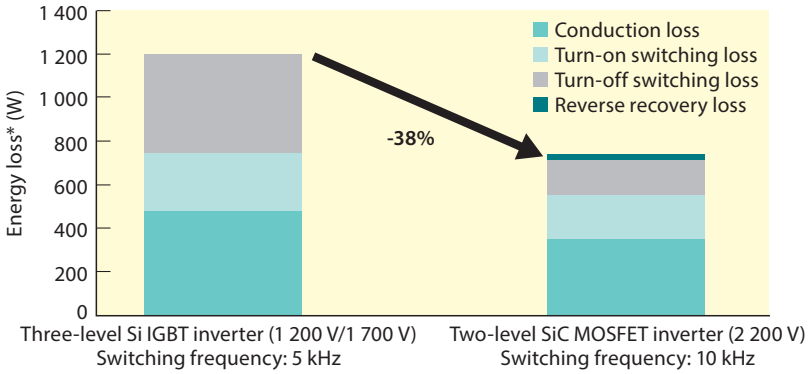
A 2 200 V, 250 A-class SiC module composed of the new SiC MOSFETs in a low-inductance standard package exhibited considerably lower switching loss than an Si module composed of Si IGBTs and Si fast recovery diode (FRDs) with the same blocking voltage. An estimate based on these results indicates that an inverter circuit with an SiC power module consumes 38% less power than one with an Si power module even when the switching frequency of SiC MOSFETs is increased to twice that of Si IGBTs. This makes it possible to reduce the size and weight of passive devices in filter circuits as well as cooling components such as heat sinks.



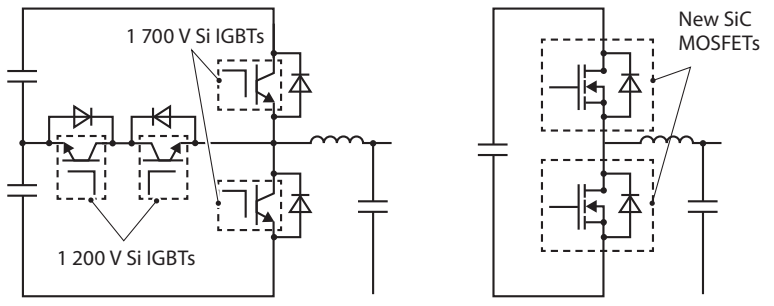
p+: p-type semiconductor with high doping concentration
n+: n-type semiconductor with high doping concentration

(a) Cross-sectional view of new SiC MOSFET

Cross-sectional view of new 2 200 V SiC MOSFET



(b) Energy loss



(c) Conventional three-level Si IGBT inverter (d) New two-level SiC MOSFET inverter

* Comparison based on electrical characteristics data published in March 2023

Comparison of power dissipation of inverters composed of conventional and new devices

4.2 Bayesian Optimization Technique to Reduce Noise and Thermal Resistance of Power Modules

SiC power devices are replacing conventional Si devices because SiC devices support higher switching frequency and load current. In line with this, there is increasing demand for packages with lower thermal resistance and noise.

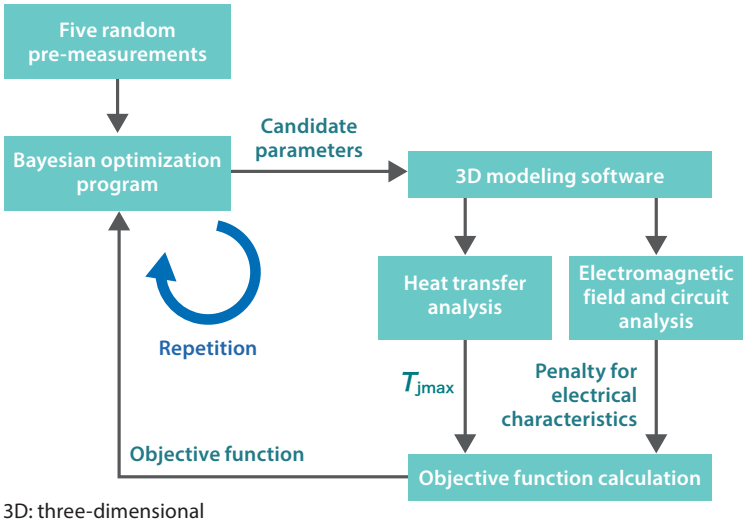
In 2020, Toshiba Electronic Devices & Storage Corporation developed an SiC MOSFET module in a standard 2-in-1 package. We have now introduced Bayesian optimization for designing a next-generation power module with improved electrical characteristics. Bayesian optimization involves repeated simulations to find the optimal package dimensions that satisfy desired electrical characteristics. Specifically, Bayesian optimization is performed to minimize the objective function that expresses package design parameters. To improve power module heat dissipation, Bayesian optimization uses the maximum temperature of an SiC chip (T_{jmax}) as the minimization target, which is determined via steady heat transfer simulation under constant heat generation. Because the new SiC MOSFET module is housed in a 2-in-1 package, we defined an objective function as the sum of the T_{jmax} values for cases where high and low arms generate heat independently and simultaneously.

Furthermore, to prevent electrical characteristic deterioration, the objective function takes into account the inductance between main terminals, parasitic resistance, current balance within a module, and switching loss. If they exceed a pre-determined value, a penalty is added to the objective function.

We created an automation program for various simulations and Bayesian optimization. The optimization process succeeded in deriving a design with lower T_{jmax} and a lower penalty on electrical characteristics than the initial design.

We prototyped a power module with the optimized design and measured its structure function to calculate thermal resistance, resulting in 0.042 K/W, approximately 16% lower than the 0.050 K/W of the conventional package.

We will continue to further improve the electrical characteristics of power modules using Bayesian optimization.



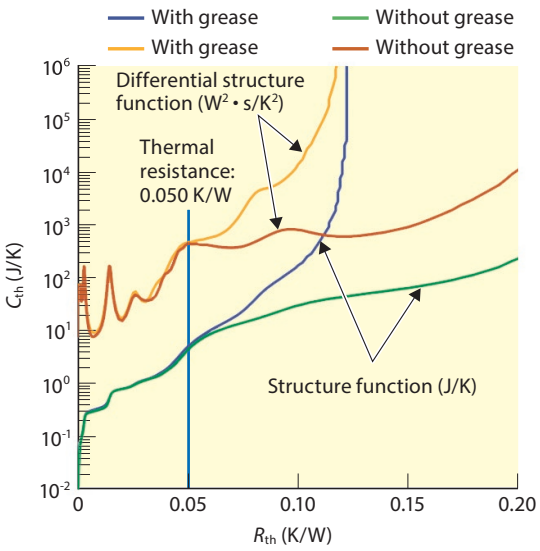
3D: three-dimensional

Bayesian optimization flowchart

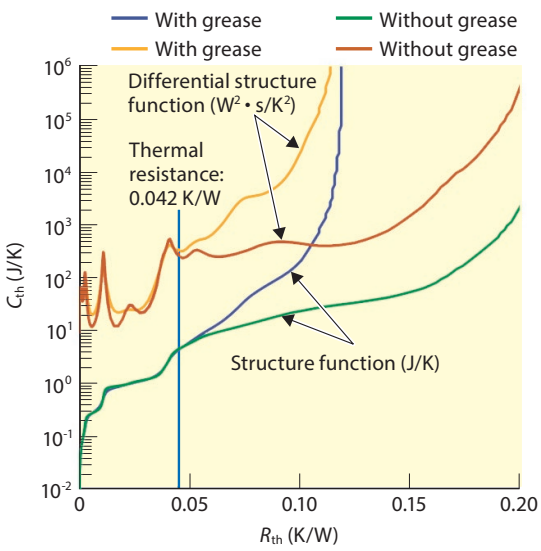
Sample module appearance

Design	T_{jmax} (°C)			Penalty for electrical characteristics	Objective function
	Both arms	High-side arm	Low-side arm		
Initial design	125.1	80.8	78.9	0.546	3.54
Optimal design	123.9	80.4	78.7	0.033	3.01

Comparison of thermal and electrical characteristics before and after optimization



(a) Structure function of conventional package



(b) Structure function of optimized package

R_{th}: thermal resistance C_{th}: thermal capacitance

Measured structure functions

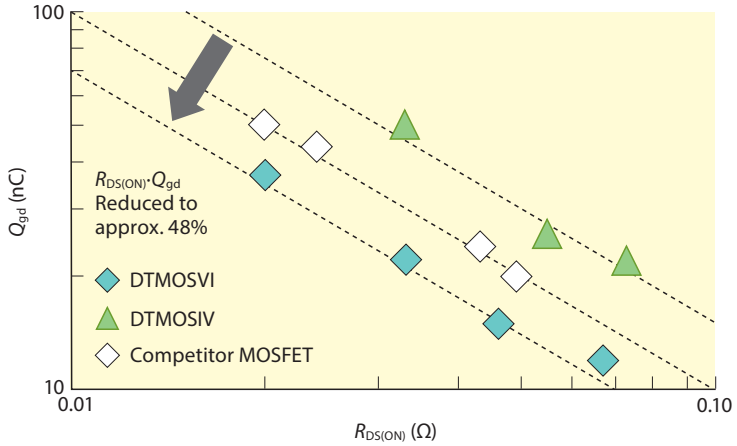
4.3 DTMOSVI 600 V Power MOSFET Series to Improve Power Conversion Efficiency

600 V DTMOSVI series MOSFET in TOLL package

Parameter		Existing DTMOSIV series	Newly developed DTMOSVI series
V_{DSS}	(V)	600	600
R_{ON}·A*	(%)	100	**84**
$R_{DS(ON)}$·Q_{gd}*	(%)	100	**48**

TOLL: Transistor Outline (TO)-Leadless
V_{DSS}: maximum rated drain-source voltage
R_{ON}·A: drain-source on-resistance per area
∗ Relative value

Comparison of figure-of-merit between existing DTMOSIV series and new 600 V DTMOSVI series super-junction power MOSFETs (SJ-MOS)



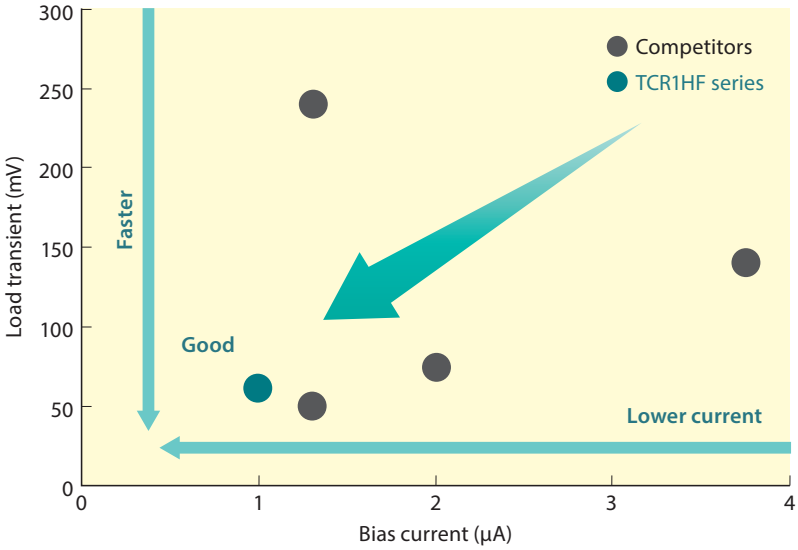
Comparison of figure-of-merit tradeoff among SJ-MOS products

To achieve carbon neutrality, efforts are being accelerated to reduce the power consumption of power supplies for industrial equipment such as data center equipment, servers, and communication base stations. Low-loss power semiconductor devices are required to improve power conversion efficiency and thereby the power efficiency of industrial equipment.

To meet this requirement, Toshiba Electronic Devices and Storage Corporation has developed the DTMOSVI series of n-channel power MOSFETs with a rated drain-source voltage (V_{DSS}) of 600 V fabricated using the latest super-junction process. We modified its gate structure to increase the switching speed while optimizing the super-junction structure to reduce the drain-source on-resistance ($R_{DS(ON)}$). Thanks to reduced switching loss and on-resistance, the DTMOSVI series exhibits a 48% lower $R_{DS(ON)}\cdot Q_{gd}$ (a performance index that indicates the power supply efficiency) than the existing product series.

We will expand the lineup of the DTMOSVI series with different on-resistance and packaging options to help further reduce the power consumption of power supplies, contributing to achieving a sustainable society.

4.4 TCR1HF Series High-Performance Linear Regulators for Battery-Powered Industrial Systems



Bias current-vs-load transient characteristics of TCR1HF series linear regulator ICs at 0 mA to 10 mA

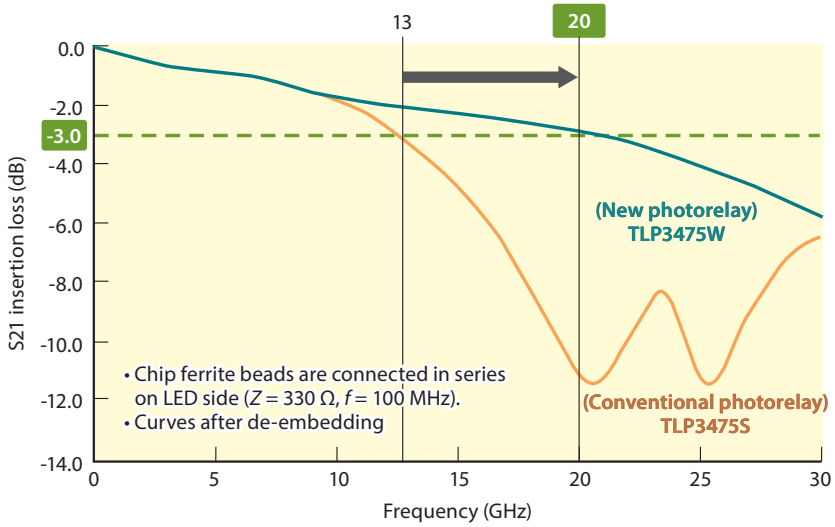
Driven by the popularity of battery-powered industrial systems, demand is increasing for those that draw minimal quiescent current most of the time and run on high current only during active operation to extend battery life.

Linear regulators, which supply power to such systems, require not only low quiescent current but also high responsiveness to deliver high current instantaneously according to load requirements.

Toshiba Electronic Devices & Storage Corporation has released the TCR1HF series of linear regulators which incorporate a new high-voltage reference current circuit to meet these requirements, achieving the industry's lowest standby current of only 1 μA(*). In addition, an ultralow-power circuit capable of sensing an output voltage dip provides superior responsiveness, ensuring that the current supply tracks load fluctuations. These technological enhancements allow for a balance between two conflicting requirements: extended life due to low-power operation and stable performance due to rapid response. Furthermore, the TCR1HF series supports a wide input voltage range of 4 V to 36 V and thus contributes to the advancement of various battery-driven industrial systems.

(*) As of May 2023, in comparison with existing products (according to Toshiba Electronic Devices & Storage Corporation research)

4.5 Compact Photorelay with Enhanced High-Frequency Characteristics



S21: Insertion loss expressed with S-parameter matrix, which characterizes HF electronic circuits
Z: Impedance
f: frequency

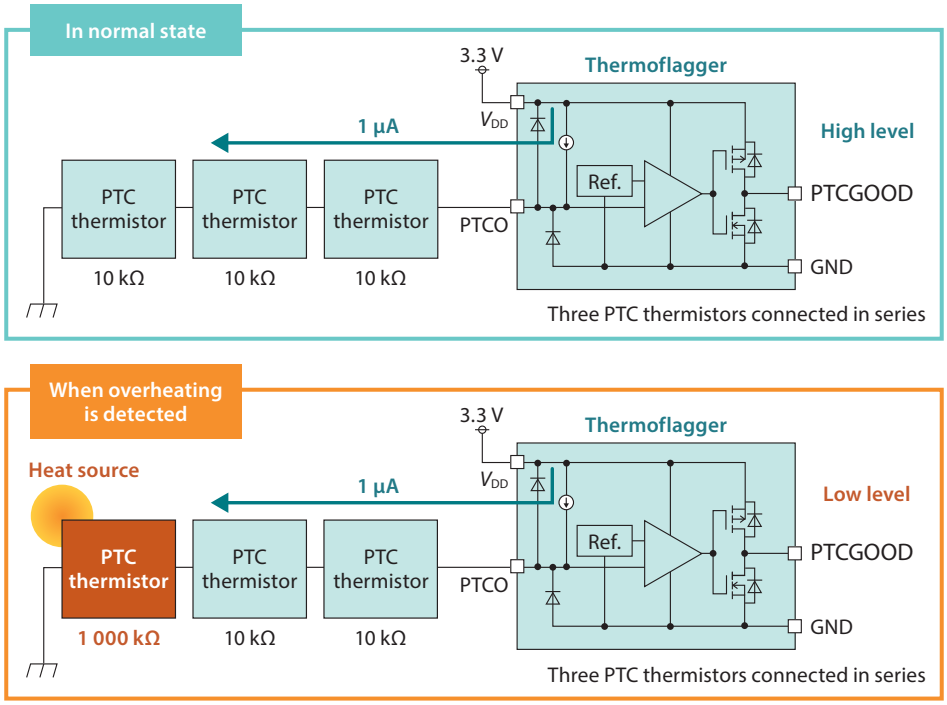
Comparison of insertion loss characteristics of new TLP3475W and conventional TLP3475S photorelays

Photorelays with excellent high-frequency (HF) and high-speed switching characteristics are required for semiconductor automated test equipment (ATE) to switch test signals, as devices under test (DUTs) are becoming increasingly versatile and fast. To deal with this, Toshiba Electronic Devices & Storage Corporation has developed the TLP3475W photorelay. It is housed in an optimized package to reduce parasitic capacitance and inductance which affect photorelay HF characteristics. The TLP3475W provides a typical critical frequency of 20 GHz (i.e., the frequency at which the insertion loss is 3 dB), which is 1.5 times higher than the 13 GHz critical frequency of the existing photorelay. Furthermore, the TLP3475W provides a 50% shorter turn-on time than the existing photorelay and thus helps to reduce the switching time of ATE signals. The TLP3475W is housed in the industry's smallest WSON4 package with a typical thickness of 0.8 mm(*), which is 40% smaller than the conventional S-VSON4T package.

We will continue developing photorelays that help to improve ATE performance and DUT measurement efficiency.

(*) As of January 2024 (according to Toshiba Electronic Devices & Storage Corporation research)

4.6 TCTH0 Series Thermoflagger Overtemperature Detection ICs



V_{DD}: power supply pin Ref: reference voltage source GND: Ground pin

Example of Thermoflagger operation

In recent years, the safety of electronic devices has become a critical concern, resulting in increased demand for robust thermal monitoring solutions.

With this in mind, Toshiba Electronic Devices & Storage Corporation has developed the TCTH0 series of Thermoflagger ICs, which are used in combination with multiple positive temperature coefficient (PTC) thermistors connected in series to detect overheating conditions at multiple locations on a circuit board.

The resistance of PTC thermistors increases abruptly at a certain temperature. The Thermoflagger IC incorporates a high-precision current source and a comparator to detect changes in resistance and indicates overheating via the PTCGOOD output pin.

PTC thermistors with a desired critical temperature can be selected arbitrarily. Quantity and board placement can also be determined arbitrarily, considering system constraints. Combined with PTC thermistors, a single piece of the Thermoflagger IC allows detection of overheating conditions at multiple board locations. This configuration helps ensure safety and reduce the cost of various system applications.

4.7 3.5-Inch Nearline HDD Using Hybrid SMR Technology

MH10F series hybrid-SMR 3.5-inch nearline HDD

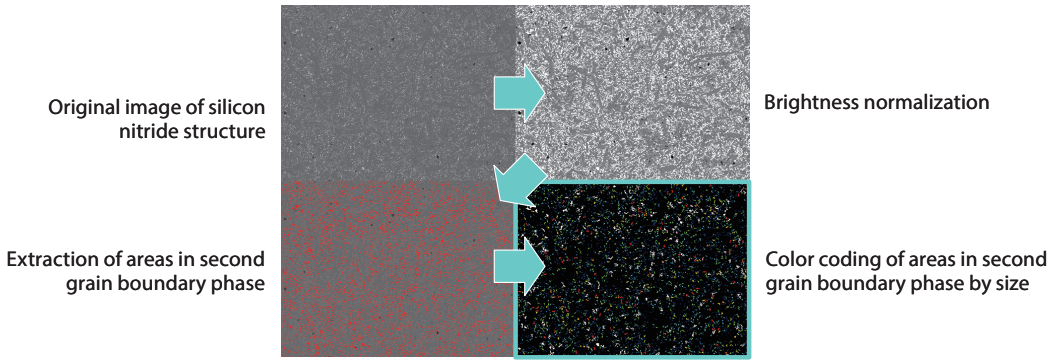
At present, data centers, which use the greatest number of hard disk drives (HDDs), emphasize a balance between performance improvement for a better user experience and capital investment for revenue optimization, requiring flexible storage operations to maintain an optimal balance. To meet the needs of data centers, the HDD industry has proposed hybrid-shingled-magnetic-recording (SMR) HDDs that combine conventional magnetic recording (CMR) optimized for performance and SMR optimized for storage capacity.

With this in mind, Toshiba Electronic Devices & Storage Corporation has developed the MH10F series of 3.5-inch hybrid-SMR nearline HDDs. This series is compliant with Zoned Device Advanced Technology Attachment (ATA) Command Set-2 (ZAC-2), an industry standard for hybrid SMR, and allows users to dynamically select CMR or SMR for each zone. This means that users can selectively use the performance optimized CMR method for more frequently accessed data to reduce the response time to user queries and improve the user experience. In addition, the MH10F series makes it possible to dynamically increase a system's overall storage capacity by setting up an SMR area for less frequently accessed data and moving sequential data to the SMR area. The MH10F series has a storage capacity of 22 terabytes (TB)(*) when all its zones are configured for CMR mode and a storage capacity of 24 TB when configured for SMR mode.

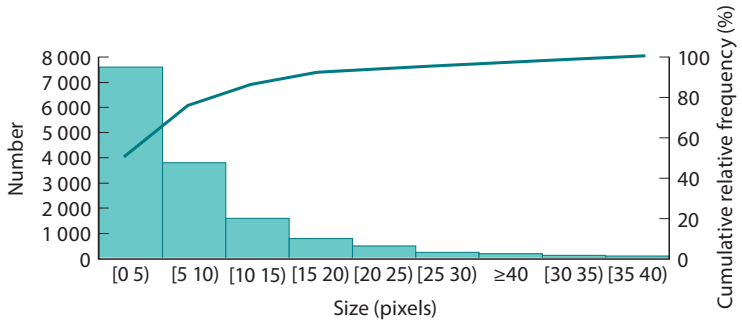
We will continue to contribute to the ever-growing storage market by offering products that can flexibly meet diverse customer needs.

(*) Definition of capacity: Toshiba Electronic Devices & Storage Corporation defines a terabyte as 10^{12} (1 000 000 000 000) bytes.

4.8 MI-Based Material Development Efforts



(a) Area extraction



[x y): From x (inclusive) to y (exclusive)

(b) Second grain boundary phase size distribution

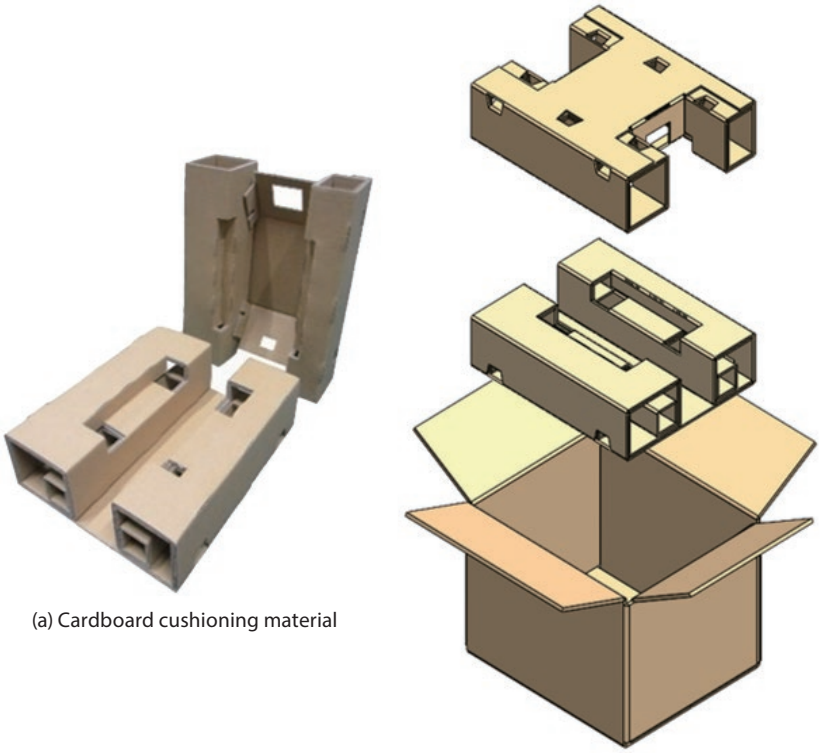
Area extraction of second grain boundary phase via image analysis and size distribution

Materials informatics (MI) techniques have attracted much attention as an innovative approach to material development which helps reduce development times and costs significantly. MI leverages large datasets and simulations to narrow down material parameters swiftly and efficiently.

Toshiba Materials Co., Ltd. is collaborating with Toshiba Corporation's Corporate Research and Development Center to establish theoretical guidelines by analyzing the correlations between material structures and properties using MI. In this endeavor, we employed proprietary image analysis techniques to numerically characterize the structures of silicon nitride materials that are expected to see increased demand. This enabled us to quantify essential structural factors that play critical roles in determining silicon nitride properties, including the distribution of particle size and second grain boundary phase size, which reveal their relationships with material characteristics. At present, we are using this knowledge as a guide for further material development.

We will continue to explore the new analysis methods as they are applicable to various materials, including ceramics and metals.

4.9 Reducing Environmental Impact of Industrial Magnetron Packaging via Design for Logistics (DFL)



(a) Cardboard cushioning material

(b) Packaging box

Example of reducing environmental impact of industrial magnetron packaging via design for logistics (DFL)

Industrial magnetrons are precision instruments which have traditionally been packaged in boxes with plastic cushioning materials to absorb shocks during transportation. However, product packaging using plastic poses environmental concerns and increases the workload due to increased package volume and weight.

With this in mind, Toshiba Hokuto Electronics Corporation has fully reviewed packaging specifications based on the concept of design for logistics (DFL), going back to the product planning and design stages to maintain product quality and reliability. This has resulted in compact, lightweight, all-cardboard packaging boxes.

During this initiative, we collaborated with SBS Toshiba Logistics Corporation, relying on their extensive logistics expertise. We conducted repeated trial and error testing via strength analysis simulation and drop impact evaluation in pursuit of the optimal packaging design. The new environmentally sustainable packaging box eliminates the use of plastic while helping cut carbon dioxide (CO_2) emissions by 25% and man hours by 30%.