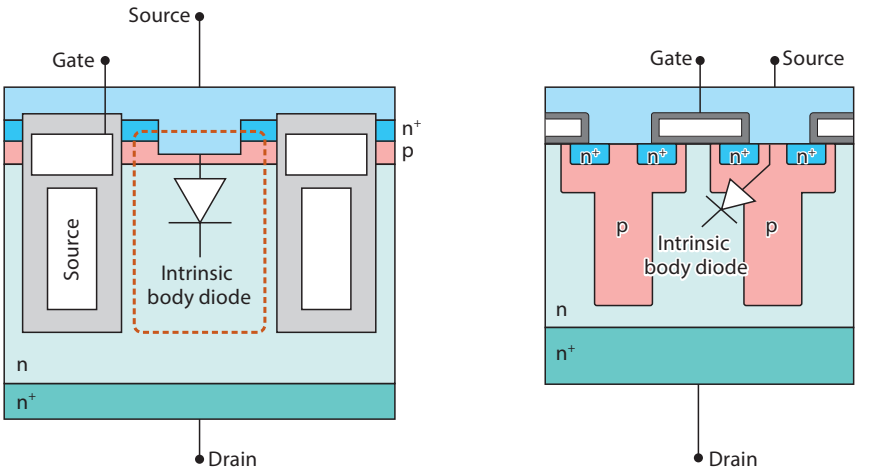
4. Electronic Devices and Storage

4.1 Power MOSFET Technology to Improve Reverse Recovery Characteristics



Cross-sectional structure of UMOSX-H 150 V power MOSFET

Cross-sectional structure of DTMOS VI 650 V power MOSFET

p: p-type semiconductor n: n-type semiconductor n^+: Highly-doped n-type semiconductor

Intrinsic body diodes in 150 V and 650 V power MOSFETs

U-MOSX-H

Item	t_{rr}	Q_{rr}
Optimized lifetime control process	40 ns	34 nC
Non-optimized lifetime control process	72 ns	130 nC
Reduction	44%	74%

Test condition Current change rate: –100 A/μs

DTMOS VI

Item	t_{rr}	Q_{rr}
Optimized lifetime control process	115 ns	0.6 nC
Non-optimized lifetime control process	330 ns	5.1 nC
Reduction	65%	88%

Test condition Current change rate: –100 A/μs

Comparison of reverse recovery time (t_{rr}), and reverse recovery charge (Q_{rr}) of power MOSFETs with conventional and new processes

Fifth-generation (5G) mobile base station power consumption is increasing due to a rise in communication traffic and growing storage capacity.

Reducing power consumption is therefore a crucial issue. To resolve this, it is necessary to improve power supply efficiency and thereby reduce power loss of the constituent power devices.

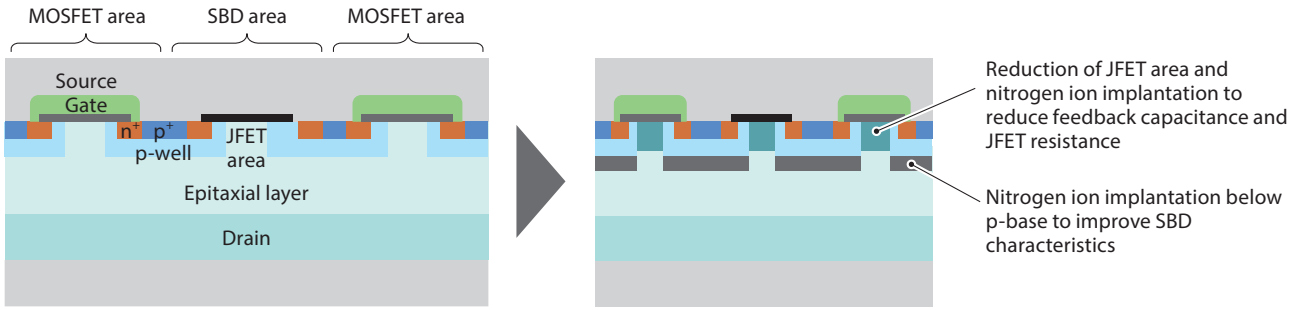
Previously, power device development focused on reducing on-resistance and gate charge. However, because on-resistance and the gate charge in modern power devices are sufficiently low, the reverse recovery loss during switching accounts for a large percentage of the total power loss. Improving reverse recovery characteristics is therefore necessary in order to further reduce the power consumption of power devices.

With this in mind, Toshiba Electronic Devices & Storage Corporation has developed a HSD (high-speed diode) series of 150 V and 650 V power metal-oxide-semiconductor field-effect transistors (MOSFETs) featuring low reverse recovery charge (Q_{rr}).

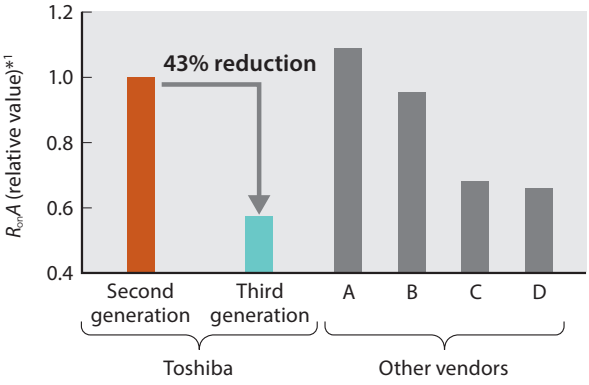
In order to reduce the reverse recovery loss of a MOSFET during switching, it is effective to reduce Q_{rr} by reducing the reverse recovery time (t_{rr}), or the time required for the carriers accumulated around the intrinsic body diode to recombine and dissipate. Therefore, we optimized the device structure by adding a lifetime control process in order to facilitate hole and electron recombination. As a result, the UMOSX-H series MOSFETs with lifetime control provide 44% lower t_{rr} and 74% lower Q_{rr} than those without it, while DTMOS VI series MOSFETs with lifetime control provide 65% lower t_{rr} and 88% lower Q_{rr} than those without it. We achieved these results without compromising the on-resistance and gate charge characteristics.

Our next step is to apply this technology to other types of power devices in order to meet future requirements for power consumption reduction and contribute to achieving carbon neutrality.

4.2 Third-Generation SiC MOSFET with Embedded SBD Combining Low Power Loss and High Reliability

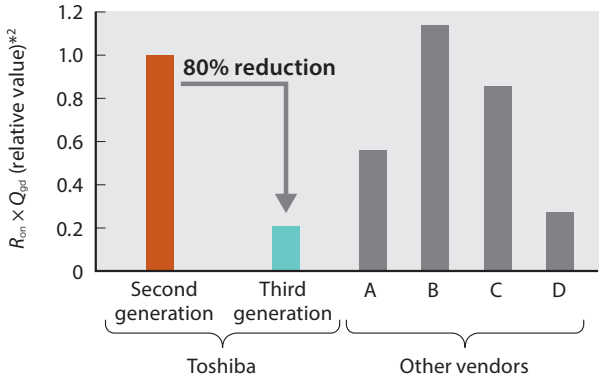


Cross-sectional structures of second- and third-generation SBD-embedded SiC MOSFETs



*1: Normalized with $R_{on}A$ of our second-generation device as 1

Comparison of specific on-resistance ($R_{on}A$) for 1.2 kV-class second- and third-generation SBD-embedded SiC MOSFETs when $R_{on}A$ of second-generation SiC MOSFET is 1



*2: Normalized with $R_{on} \times Q_{gd}$ of our second-generation device as 1

Comparison of on-resistance (R_{on}) × gate-drain capacitance (Q_{gd}) of 1.2 kV-class second- and third-generation SBD-embedded SiC MOSFETs when $R_{on} \times Q_{gd}$ of second-generation SiC MOSFET is 1

To reduce electrical equipment power consumption and help to achieve carbon neutrality, it is essential to improve power semiconductor performance. With this in mind, silicon carbide (SiC) is attracting attention as a replacement material for silicon (Si) as it improves power semiconductor performance. However, SiC has several known issues that affect device reliability. One is that when the parasitic pn diode of an SiC MOSFET conducts electricity, its energy causes the crystal defects inherent in an SiC wafer to expand, causing the MOSFET characteristics to deteriorate.

To resolve this issue, Toshiba Electronic Devices & Storage Corporation developed and released the second-generation SiC MOSFET with an embedded Schottky barrier diode (SBD). Because current passes through the SBD, the SBD-embedded SiC MOSFET restricts the operation of the intrinsic pn diode and thus reduces the expansion of inherent crystal defects.

However, the embedded SBD reduces the area that functions as a MOSFET and causes an increase in on-resistance per unit area ($R_{on}A$) and the product of R_{on} and gate-drain charge (Q_{gd}), both of which are important figures of merits (FOMs) of power MOSFETs. Therefore, the embedded SBD causes large conduction and switching losses.

As a next step, we have developed and commercialized a third-generation SiC MOSFET that combines excellent electrical characteristics and high reliability. While adopting the same structure as the second-generation SiC MOSFET, we have reduced the SBD area in the third-generation SiC MOSFET by optimizing the ion implantation profile. As a result, the third-generation SiC MOSFET has 43% lower $R_{on}A$ and 80% lower $R_{on}\times Q_{gd}$ than those of the second-generation SiC MOSFET, both which compare favorably with SiC MOSFETs from other vendors.

4.3 Universal Thermal Diffusion Model for Point Defects in SiC Power Semiconductors

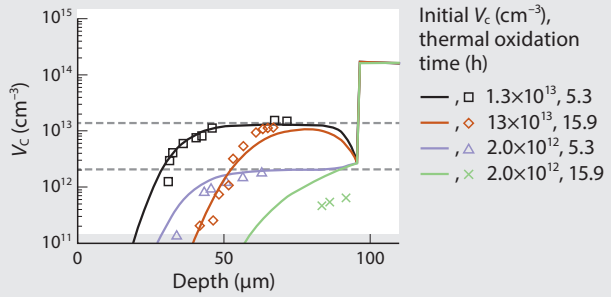
$$\frac{dV_c}{dt} = \nabla\left(\sum_z \left(D_{vc^z} \cdot \nabla(V_c^z) + \frac{q}{kT} \cdot D_{vc^z} \cdot Z \cdot V_c^z \cdot \nabla(\Psi)\right)\right) + G\text{-}R \quad (1)$$

$$\frac{dC_I}{dt} = \nabla\left(\sum_z \left(D_{ci^z} \cdot \nabla(C_i^z) + \frac{q}{kT} \cdot D_{c^z} \cdot Z \cdot C_i^z \cdot \nabla(\Psi)\right)\right) + G\text{-}R\text{-}Trapping \quad (2)$$

$$Trapping = 4\pi \cdot r_{cap,trap} \cdot C_{Trap} \cdot D_{CI} \cdot (C_I - C_{I,eq}) \quad (3)$$

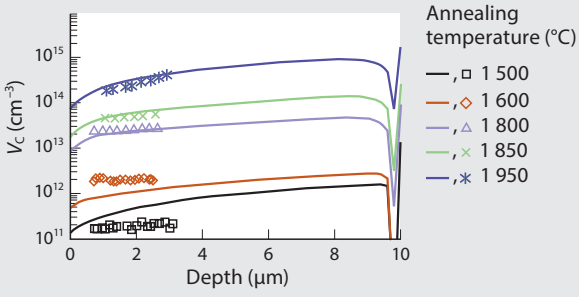
V_c: carbon vacancy density
C_I: interstitial carbon density
z: number of electric charge state instructions
D: diffusion coefficient
Ψ: potential
Q: elementary charge
k: Boltzmann constant
T: absolute temperature
G: generation rate
R: recombination rate
$r_{cap,trap}$: diameter in which Ci is captured into substrate defects
C_{Trap}: Trapping density in substrate
t: time
$C_{I,eq}$: value of C_I in equilibrium state

Calculation formulas for newly developed simulation model



* Plotted dots represent measured results while curves represent simulated results.

Comparison of measured and simulated distributions of carbon vacancies (VC) in SiC after thermal oxidation at 1 300°C



* Plotted dots represents measured results while curves represent simulated results.

Comparison of measured and simulated distributions of VC in SiC after high-temperature annealing at different annealing temperatures

Achieving carbon neutrality to mitigate global warming is a worldwide issue. SiC power semiconductor devices are expected to contribute to the improvement of power converter efficiency because of their superior electrical characteristics.

To develop semiconductor devices with a new structure, it is essential to employ technology computer-aided design (TCAD) and other simulators. However, SiC is a relatively new material, and physical models for SiC devices have yet to be fully developed.

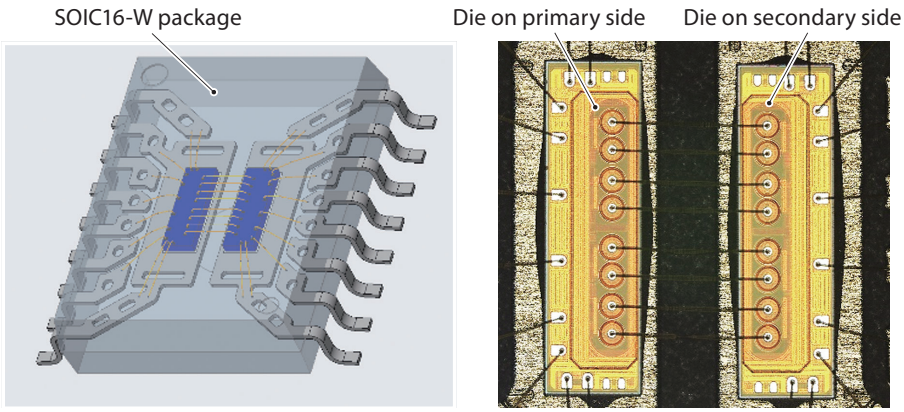
In SiC, carbon vacancies (VC) are known to exist in a stable state as point defects, which affect the electrical characteristics of the SiC device. With the aim of improving device simulation accuracy, Toshiba Electronic Devices & Storage Corporation experimented with incorporating a VC distribution model into the Sentaurus™ Process simulator. This model represents the generation, diffusion, and recombination processes of VC and interstitial carbon (Ci) atoms during thermal oxidation and activation annealing.

Previous studies proposed models for (1) thermal oxidation (at 1 150 to 1 400°C) and (2) ultrahigh-temperature activation annealing (at up to 1 950°C). However, these models are not universal because the experimental results referenced by model (1) cannot be reproduced using model (2) which covers a wider temperature range.

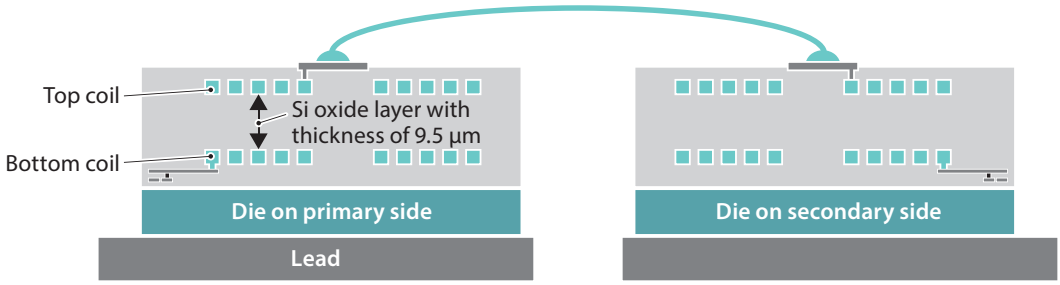
On the other hand, it is known that many types of defects exist in the SiC substrate. In this study, we developed a model, adding the term *Trapping* representing a rate of additional Ci trapping in the substrate to the Ci diffusion equation because we assumed that the defects in the SiC substrate capture some of the Ci atoms diffused from the epitaxial layer or release excess Ci atoms.

When we optimized the parameters in the new model, it successfully reproduced the experimental results referenced by models (1) and (2) with a high degree of accuracy, confirming its universality. Our next step is to develop a model for point defect generation due to ion implantation as well as an integrated simulation environment that takes the point defect distribution into consideration.

4.4 Digital Isolator with High Noise Immunity Contributing to Carbon Neutrality



(a) Perspective view of digital isolator and IC dies



(b) Cross-sectional view of isolation transformer

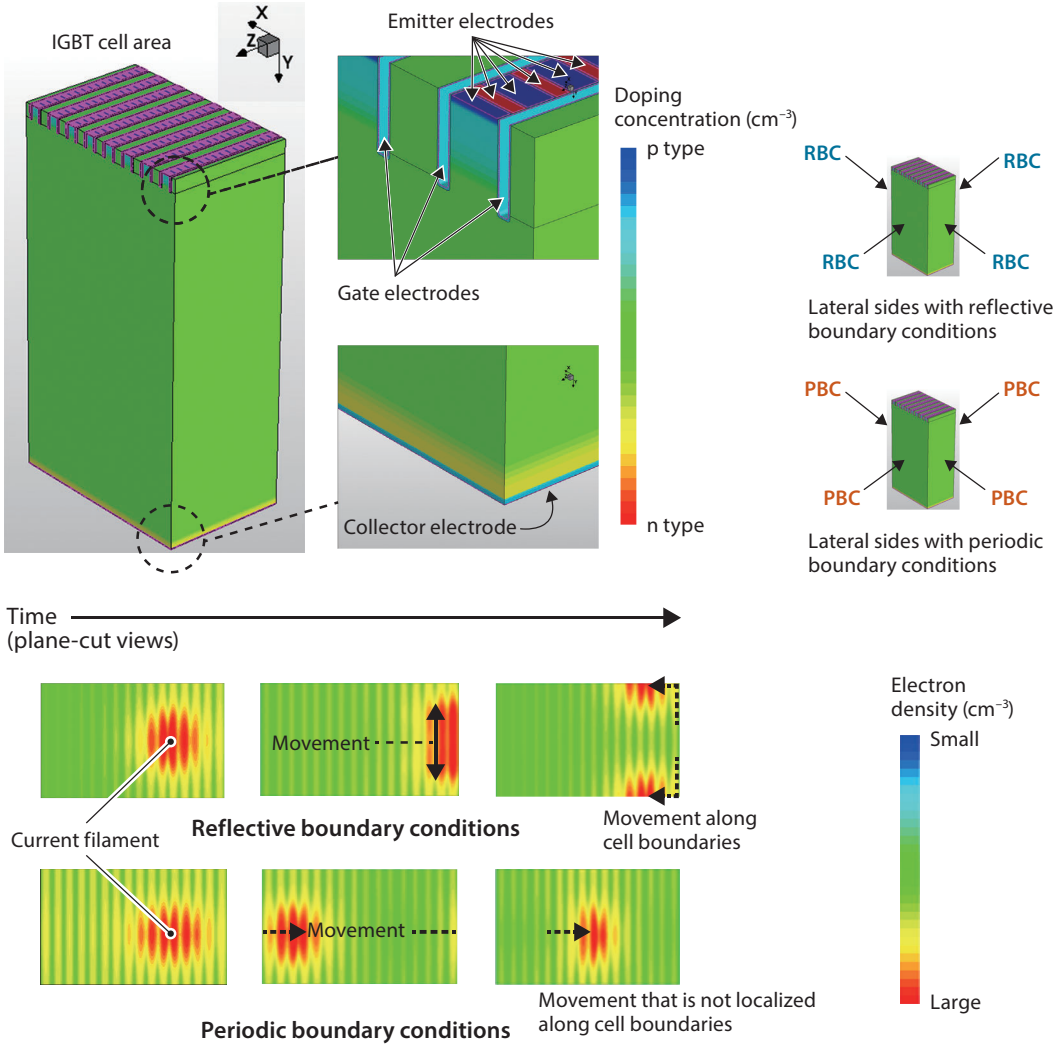
Basic structure of prototype digital isolator

As efforts to reduce greenhouse gas emissions are accelerating worldwide toward the realization of carbon neutrality, use of electric vehicles and renewable energy equipment is moving forward. The electronic boards in such devices incorporate many photocouplers to transfer electrical signals between two isolated circuits in different voltage domains and prevent transient noise from interfering with the low-voltage end. One characteristic of the photocoupler is high noise immunity, i.e., the ability to tolerate transient changes in the potential difference between two grounds on the input and output ends.

Toshiba Electronic Devices & Storage Corporation has now launched highly reliable digital isolators with a high level of common-mode transient immunity (CMTI). The new digital isolators provide an insulation voltage of 5 000 Vrms, (60 seconds), which satisfies stringent noise immunity isolation standard requirements. This is achieved by (1) forming a high-quality Si oxide layer with a thickness of 9.5 µm as an insulation layer between the coils of an isolation transformer although a Si oxide layer is typically used in the complementary metal-oxide semiconductor (CMOS) process and, (2) using a double insulation structure in which two isolation transformers are connected in cascade.

Cascading isolation transformers usually cause an increase in signal attenuation. However, the new digital isolators amplify an input signal with a high-frequency amplifier circuit to achieve full-wave rectification and envelope wave detection, thereby providing stable operation and suppressing supply current.

4.5 Development of Ultra-Large-Scale 3D Simulation Technology for Semiconductor Device Reliability Design



Current filament behavior in IGBT with ultra-large-scale 3D structure under different boundary conditions

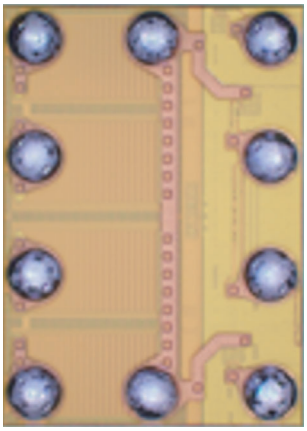
In recent years, simulation has been employed to analyze the physical behavior of semiconductor devices and thereby reduce development times. Three-dimensional (3D) simulation is desirable, particularly for insulated gate bipolar transistors (IGBTs), because they exhibit marked 3D characteristics.

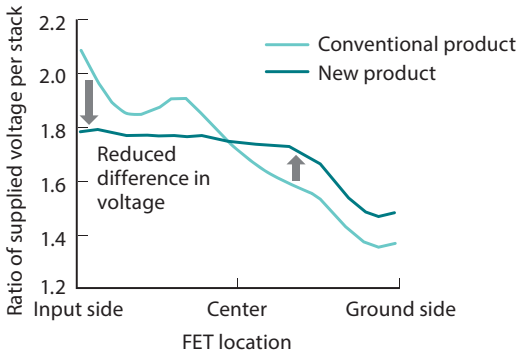
One of the most important fundamental technologies for reliability design is simulation technology for grasping the behavior of a current filament, or a localized and inhomogeneous distribution of electric current. High-density current generates Joule heating and can eventually lead to the destruction of a semiconductor device.

With this in mind, Toshiba Electronic Devices & Storage Corporation investigated the boundary conditions on the lateral sides of an IGBT which are necessary to accurately simulate the movement of current filaments in an IGBT cell using an ultra-large-scale 3D structural model.

Reflective boundary conditions (RBCs) produced an unnatural result showing current filament movement along the boundary of the IGBT cell. On the other hand, periodic boundary conditions (PBCs) resulted in a natural and reasonable movement of current filaments. Although a simulation is generally less likely to converge under periodic boundary conditions, we succeeded in improving simulation convergence by optimizing the settings of a matrix solution method.

4.6 High-Voltage RF Switch IC for Antenna Tuning Fabricated Using Latest TarfSOI Process





New TCWA0406G RF switch IC chip for mobile devices and input voltage applied to each FET in TCWA0406G

Characteristic		Required specification	Conventional product		New product
Part number		-	TCWA0403		TCWA0406G
Process		-	TaRF9		TaRF12
PH	(V)	80	84.5		91.7
R_{on}	(Ω)	2.1	2.37	*PH*: Approx. 10% increase R_{on}: Approx. 10% reduction C_{off}: Approx. 25% reduction	2.16
C_{off}	(fF)	130	178		132

f : femto (10^{-15})　　R_{on}: on-resistance　　C_{off}: off-capacitance

Comparison of main characteristics of TCWA0406G and product using conventional silicon-on-insulator (SOI) process

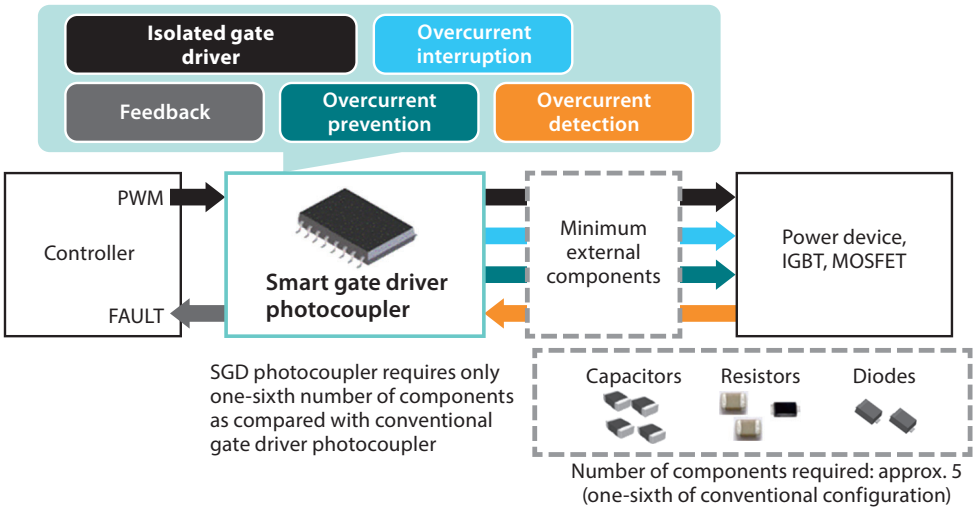
To enhance the selectivity of antennas for high-speed mobile communications such as 5G mobile networks, antenna-tuning switches are placed far away from a signal feed point. This causes an increase in voltage supplied to the switches, necessitating a power handling (*PH*) capability as high as 80 V. However, for a MOSFET fabricated using the TaRF9 process, a conventional silicon-on-insulator (SOI) process for radio-frequency (RF) switch ICs, *PH* is degraded in the high-voltage region by an increase in body leakage current (I_b).

With this in mind, Toshiba Electronic Devices & Storage Corporation has developed a new process called TaRF12, which provides a higher *PH* capability than the TaRF9 process, resulting in the TCWA0406G, a new high-voltage RF switch IC fabricated using the TaRF12 process. Because of the optimized gate length and impurity profile, the new process reduces I_b dramatically, increasing *PH*. On the other hand, because the switch is composed of multistage field effect transistors (FETs), higher voltage is applied to the FETs closer to the input terminal of the switch. To solve this problem and further increase *PH*, we performed an electromagnetic analysis to adjust the line length and reduce differences in voltage between FETs. Thanks

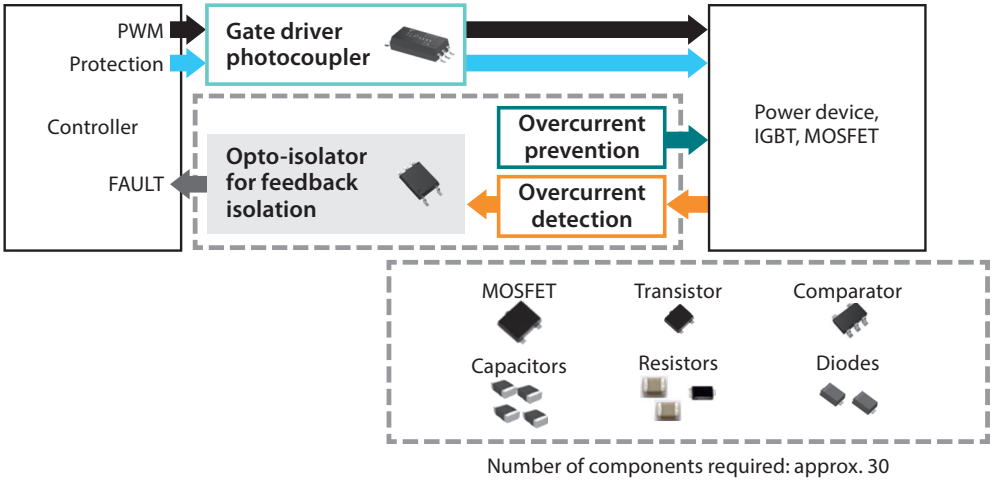
to the new process and the improved circuit design, the TCWA0406G has achieved lower on-resistance and off-capacitance than a conventional product, and a *PH* of more than 90 V.

We will further improve the TarfSOI process to develop new RF switch ICs with a supply voltage as low as 1.2 V.

4.7 Smart Gate Driver Photocoupler to Simplify Gate Drive and Protection Circuit for Power Devices



Configuration using SGD photocoupler



Configuration using conventional gate driver photocoupler

PWM: pulse-width modulation FAULT: fault output

Block diagrams of power device drive and protection circuits using smart gate driver photocoupler

Efforts are being made around the world to achieve carbon neutrality and tackle climate change. With devices for power supply applications attracting attention as one of the key enablers in carbon neutrality, the importance of gate drivers that control such devices is also increasing.

A smart gate driver (SGD) photocoupler, which is an isolated gate driver with protective functions for power devices, simplifies the design of a gate drive and protection circuit for power devices for factory automation and renewable energy applications. The SGD photocoupler requires only one-sixth the number of components to achieve the same function compared to conventional gate driver photocouplers.

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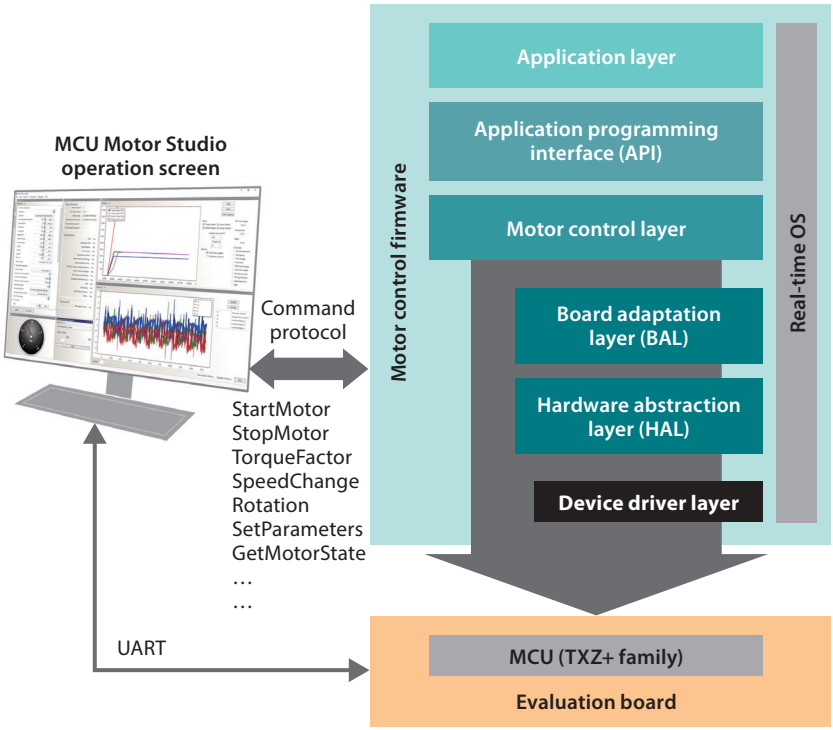
Toshiba Electronic Devices & Storage Corporation has launched the TLP5222 SGD photocoupler, which supports automatic recovery from protective operation, eliminating the need for recovery control. The TLP5222 further simplifies circuit design. Customers can now select a gate drive photocoupler that best suits their needs from conventional photocouplers such as the TLP5212 and TLP5214A, and the new SGD photocoupler, depending on the application usage environment and design concept.

4.8 MCU Motor Studio for Motor Control System Development



OS: Operating system UART: Universal Asynchronous Receiver/Transmitter

Configuration of MCU Motor Studio motor control system development environment

In May 2022, Toshiba Electronic Devices & Storage Corporation released MCU Motor Studio, a software development environment for the motor control microcontroller unit (MCU). It is an easy-to-use motor control solution and allows development environment setup simply by connecting a PC and an evaluation board with a Universal Serial Bus (USB) cable.

To develop vector control applications, it is necessary to check motor operation while adjusting control parameters. MCU Motor Studio consists of two main components: a PC tool for motor control and motor control firmware. Equipped with an intuitive graphical user interface (GUI), the PC tool for motor control allows control parameters to be adjusted while monitoring internal states and supports motor drive control, real-time logging, and diagnosis without modifying the software. The motor control firmware is scalable and fully configurable; therefore, it supports a wide range of our MCUs and evaluation boards. We are planning further updates to support more MCUs and evaluation boards and add new enhancements.

4.9 3.5-Inch 20 Tbyte Nearline HDD Series Achieved with 10 Platter Stacking Technology

MG10 series 20 Tbyte 3.5-inch nearline HDD

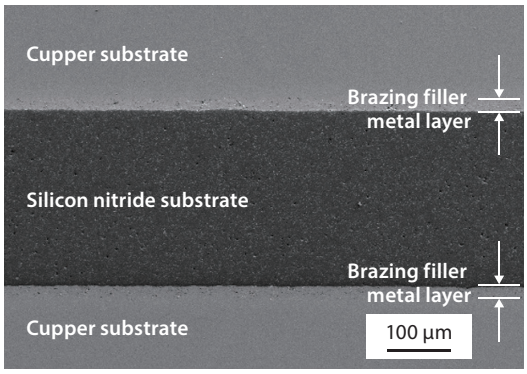
Demand for high-capacity nearline hard disk drives (HDDs) has increased accompanying recent data center expansions to accommodate the massive amount of stored corporate and personal information. Following the MG09 series of 18 Tbyte (T: tera = 10^{12}) HDDs containing nine stacked platters, Toshiba Electronic Devices & Storage Corporation has developed and launched the MG10 series of 10-platter 20 Tbyte HDDs.

Reducing the platter thickness may have been an easy way to achieve a 10-platter stack, but we chose to use the MG09 series platters on the MG10 series as HDD performance evaluation indicated that the basic stacking technology we have developed can be adapted for the MG10 series.

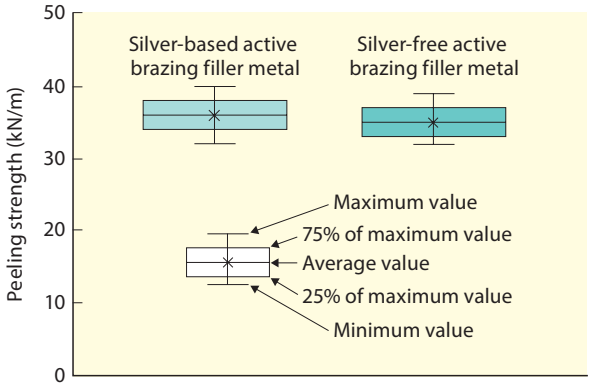
To achieve a 10-platter HDD, it was necessary to develop and verify new technologies to allow sufficient spacing between platters and maintain power consumption and HDD performance. We ensured spacing between platters by designing smaller printed circuit boards and overlapping the vertical positions with the platters. In addition, we optimized the motor bearing and housing design to suppress an increase in motor current and power consumption due to a higher number of rotating platters. Furthermore, in order to maintain HDD performance, we reduced the thickness of the arm extending to the read/write head so that the higher number of read/write heads does not result in heavier moving parts and thus an increase in access time. The combination of these technologies has successfully resulted in a ten-platter 20 Tbyte 3.5-inch nearline HDD with the same performance as the previous series.

The expansion of a data-driven society is expected to spur further demand in HDD capacity requirements. We will continue to further develop platter-stacking technology as we believe further platter stacking will be necessary.

4.10 Silver-Free Brazing Filler Metal for Insulated Circuit Boards with Copper Circuits Formed on Silicon Nitride Ceramic Substrate



Cross-sectional structure of brazed sample when applying silver-free active brazing filler metal to copper-silicon nitride (Cu-Si_3N_4) substrate



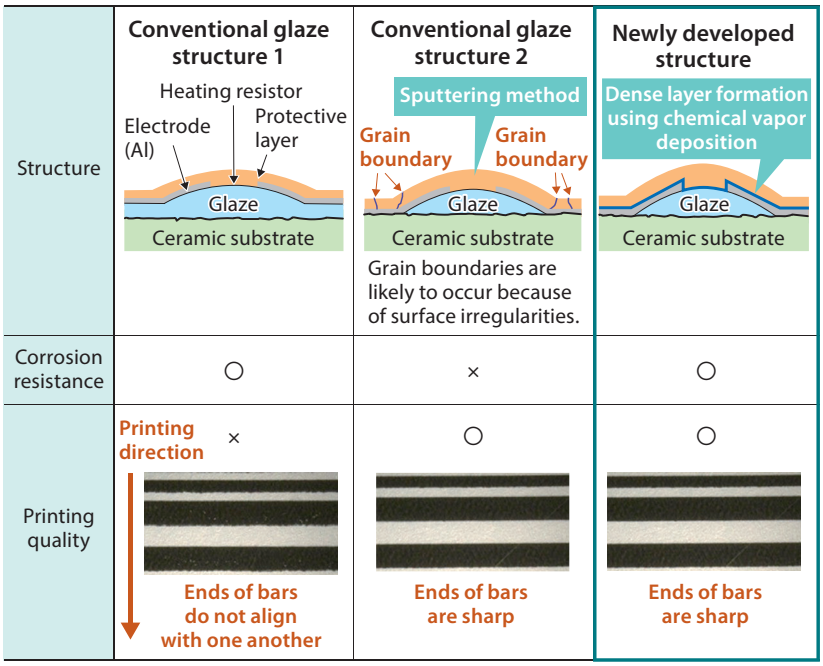
Comparison of peel strength on brazed samples using silver-based and silver-free active brazing filler metals

In recent years, demand for insulated circuit boards on power modules has grown rapidly, mainly for automotive power semiconductor applications. Insulated circuit boards consist of copper circuits formed on a silicon nitride ceramic substrate with excellent heat dissipation properties and strength. Because the insulated circuit board must have excellent strength and a heat resistance cycle, an active metal brazing method using silver-based brazing filler metals has conventionally been used as they have superior wettability and form strong bonds with silicon nitride. However, because silver is a precious metal, it is difficult to reduce insulated circuit board costs.

To resolve this issue, Toshiba Materials Co., Ltd. has developed a silver-free active brazing filler metal. By optimizing the alloy composition and the bonding process, it is possible to uniformly wet the surface of the new brazing filler metal and spread it on a silicon nitride substrate. This makes it possible to form high-strength bonds without defects and achieve characteristics equivalent to a material bonded using a silver-based brazing filler metal.

The new technology helps not only to reduce the costs of insulated circuit boards but also environmental impact as they use less rare metal. Currently, we are developing manufacturing technology to achieve practical applications for silver-free brazing filler metal.

4.11 Thermal Print Head Print Quality Improvement for Barcode Printers



Al : aluminum

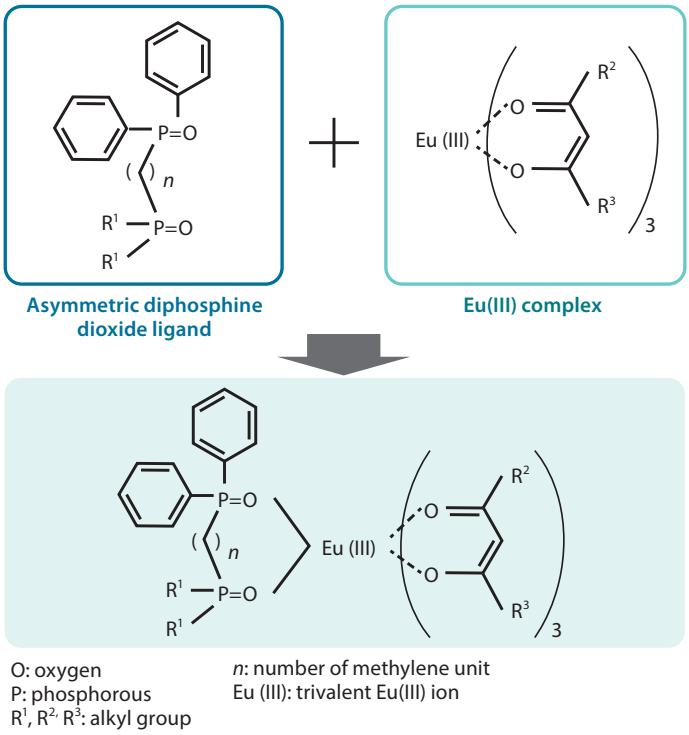
Comparison of vertical barcode images printed using partial etching glaze (PEG) and the new substrates for thermal print heads

A thermal print head (TPH) is an electronic device that uses Joule heat generated by resistors to print images on print media. Demand for barcode printers has continued growing in the distribution market in line with ever-increasing online shopping.

Printing quality and corrosion resistance are important for barcode printer TPHs. Printing quality is affected by the heat responsiveness of and the pressure applied to the TPH, and both printing quality and corrosion resistance depend on the type of glazed substrate used and protective layers. Conventionally, only a sputtering technique has been used to form protective layers. However, in the case of conventional sputtering techniques, there is a trade-off relationship between printing quality and corrosion resistance. Even if a glazed substrate with high level of corrosion resistance is used, sputtering does not provide satisfactory printing quality on a glazed substrate.

To overcome this, Toshiba Hokuto Electronics Corporation has formed a dense layer at the bottom of the protective layers using chemical vapor deposition while forming the top protective layer using a conventional sputtering technique. As a result, we have succeeded in developing a TPH with excellent printing quality and high corrosion resistance. The mass production of the TPH began in August 2022.

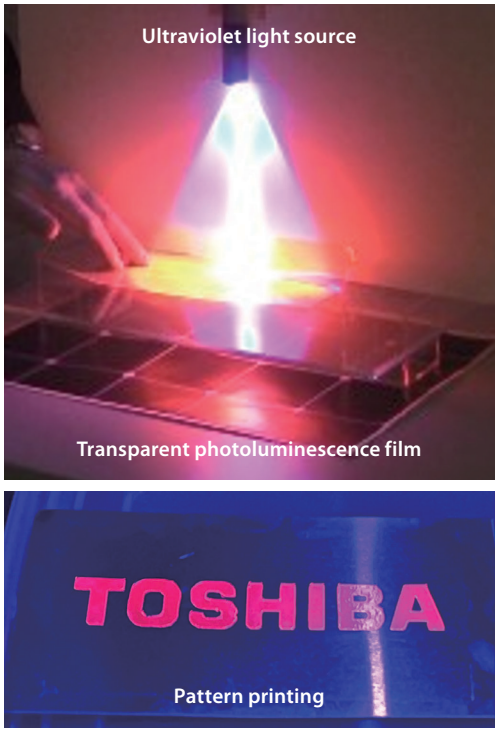
4.12 Transparent Photoluminescence Materials Suitable for Various Applications



O: oxygen
P: phosphorous
R^1, R^2, R^3: alkyl group

n: number of methylene unit
Eu (III): trivalent Eu(III) ion

Molecular structure of novel luminescent complex with asymmetric diphosphine dioxide ligands



Transparent photoluminescence under ultraviolet irradiation

Transparent photoluminescence materials, which consist of lanthanide complexes and polymers or solvents, are colorless under indoor lighting and emit a pure red color when irradiated with ultraviolet (UV) light, making them promising candidates for display and security applications.

In 2003, Toshiba Corporation found that the coordination of two different phosphine oxide structures to one europium(III) (Eu(III)) ion is effective in increasing the photoluminescence intensity and solubility of lanthanide complexes. Since then, we have been working on many novel Eu(III) complexes based on this concept.

We have optimized our original molecular design concept for Eu(III) complexes, or more specifically, the coordination of a specific asymmetric diphosphine dioxide ligand with an Eu(III) ion. We have developed new, highly soluble Eu(III) complexes that produce a stronger red emission by coordinating the asymmetric diphosphine dioxide ligand. These Eu(III) complexes are easy to process into ink or films compared with previously reported Eu(III) complexes. The new Eu(III) complexes are excitable by light across a wide wavelength from deep UV to purple to obtain stronger red emissions and excellent visibility. Because of this feature, the new Eu(III) complexes show promise in the following applications:

(1) Micro-light-emitting diode (LED) displays have attracted much attention as a next-generation display in recent years. The application of transparent photoluminescence materials to micro-LED displays provides both color purity (i.e., the resemblance of color to its hue) and display brightness.
(2) Because the new Eu(III) complexes are easy to process into an ink for inkjet printing, they can be used to prevent banknote counterfeiting, passports, entrance tickets, works of art, etc.
(3) Although 222-nm deep UV light can be used to deactivate viruses with little adverse effects on the human body, it is totally invisible. The area irradiated by UV light can be made visible by converting UV light into red light.

Dichlorvos is widely used as an effective pesticide, but it is highly toxic to humans. We found that the photoluminescence quenching phenomenon of an Eu(III) complex can be used to detect dichlorvos.

With the aim of commercializing transparent photoluminescence materials, we are currently conducting a proof-of-concept (POC) experiment to validate customer needs.