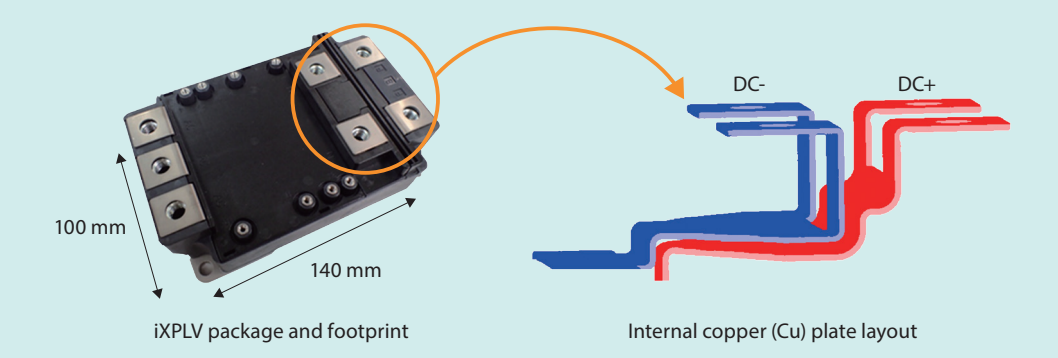
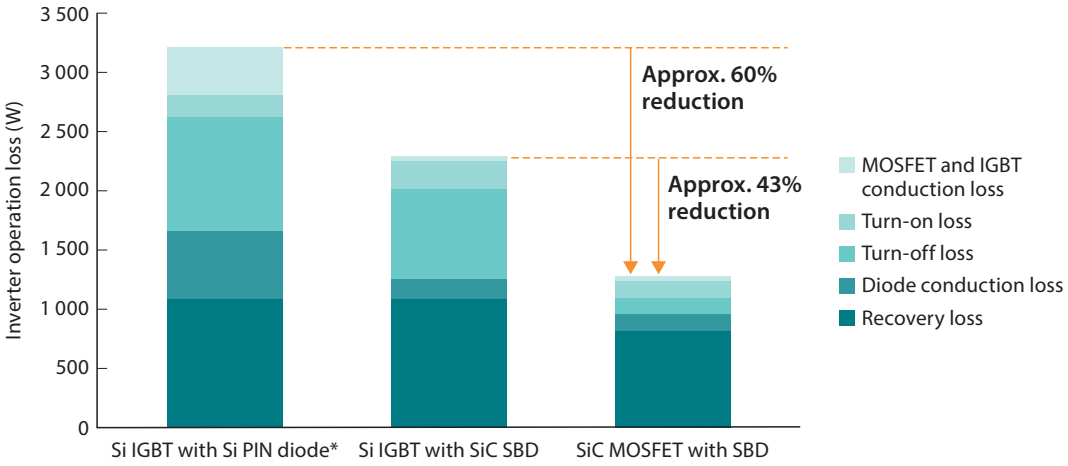
4. Electronic Devices and Storage

4.1 Highly Reliable and Compact SiC Power Module



iXPLV package for SiC MOSFETs and internal structure of electrodes



Conditions
Drain-source voltage: 1 500 V Drain current: 1 024 A Load power factor: 0.85
Switching frequency: 1 kHz Junction temperature: 150°C

*PIN diode: a diode with an intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor

Comparison of power dissipation in conventional Si IGBT and newly developed SiC MOSFET modules during inverter operation

Toshiba Electronic Devices & Storage Corporation has developed a highly reliable and compact silicon carbide (SiC) power module, which helps to reduce the size and weight and increase the energy efficiency of power conversion systems.

Conventional SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) are susceptible to degradation of electrical characteristics due to the expansion of crystal defects when the body diode conducts. To solve this problem, we developed SiC MOSFETs with a Schottky barrier diode (SBD) and commercialized 1.2 kV-class devices. We have now developed third-generation SiC MOSFETs with an optimized structure that provide higher blocking voltage, higher reverse current-carrying capacity, and lower loss than the second-generation devices. The newly developed 3.3 kV-class device has a specific on-resistance of 12.4 $m\Omega \cdot cm^2$ at room temperature, 20% lower than the 15.5 $m\Omega \cdot cm^2$ of the previous device.

Furthermore, we have developed a new package called iXPLV (Intelligent fleXible Package, Low Voltage) utilizing the high-speed advantage of SiC. In addition to an approximately 23% smaller footprint than a conventional package with the same current rating, the iXPLV package provides an internal module inductance of 12 nH, down from 20 nH, because of the optimized internal electrode structure. Moreover, instead of the conventional solder bonding, the iXPLV package is assembled using silver sinter bonding to bond the SiC chip to a copper substrate. As a result, the power cycling capability of the iXPLV package is more than double that of the conventional package.

We combined the newly developed SiC MOSFET chip and the iXPLV package to develop a 3.3 kV, 800 A-class SiC power module. This SiC module makes it possible to reduce the operating loss of an inverter by roughly 60% in comparison with our conventional silicon (Si) insulated-gate bipolar transistor (IGBT) module. The new SiC module can use an approximately 59% smaller heatsink and thus helps to reduce the size and weight of a power conversion system.

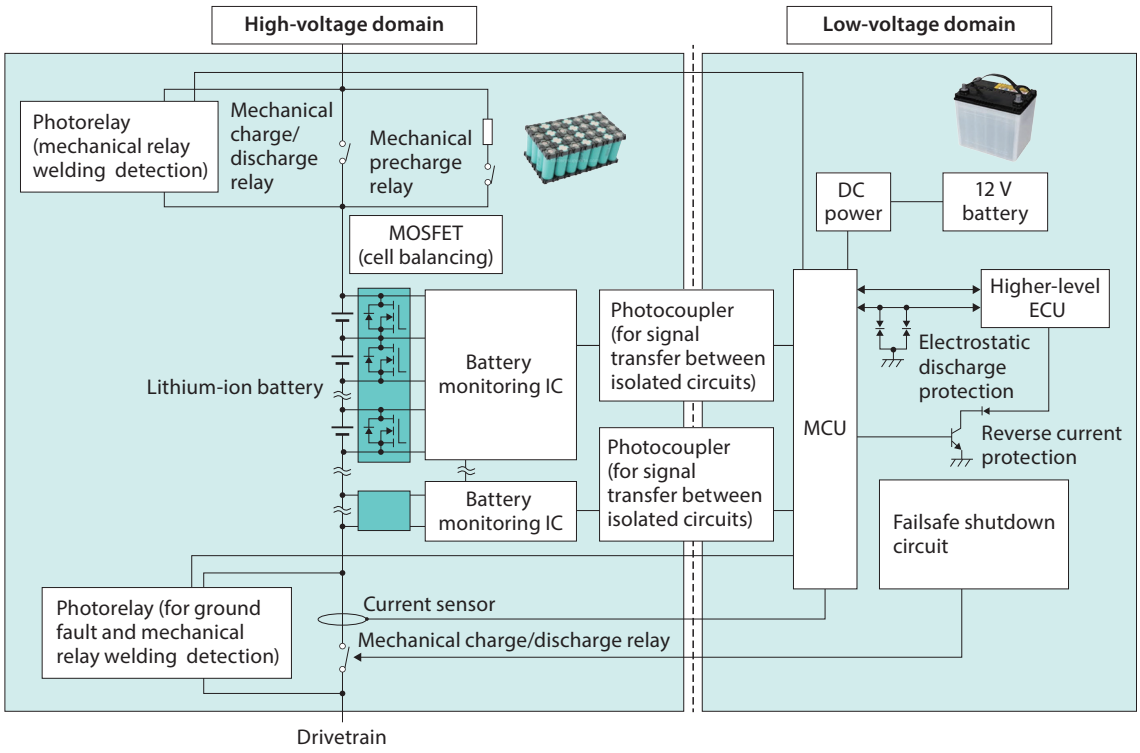
4.2 1 500 V Photorelay for Automotive BMS

Many countries and regions have been tightening automotive environmental regulations in recent years to alleviate global warming and air pollution. Automakers are accelerating the introduction of green vehicles such as hybrid electric vehicles (HEVs) and electric vehicles (EVs) to comply with the ever-tightening environmental regulations.

In order to extend the per-charge travel distance and shorten the charging time, the driving battery voltage for green vehicles is being increased from 400 V or less and will reach up to 1 000 V in the future. It is therefore required to increase the voltage of automotive battery management systems (BMS) for efficient use of batteries. High voltage is also required for photorelays that are used in the BMS to detect ground faults and the welding of mechanical relays.

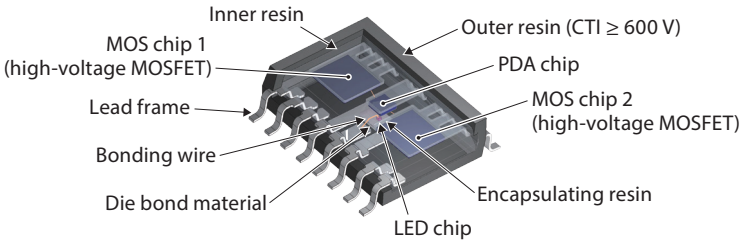
Under these circumstances, Toshiba Electronic Devices & Storage Corporation has developed a new high-voltage photorelay for BMS applications. The newly developed photorelay is sealed in a package with double-molded resin to reduce internal thermal stress. Double-molding is a heat resistance technology that we have cultivated through the development of automotive technologies. In addition, the new package is designed using appropriate materials in compliance with pollution degree 2 and material grade I of the International Electrotechnical Commission (IEC) 60664-1 standard while maintaining a height of only 2.55 mm.

In order to increase the withstand voltage of the BMS, we have also developed a 1 500 V MOSFET by optimizing the distribution of electric field strength around the edges of the chip when voltage is applied, drawing on our power device design and process technologies. The newly developed photorelay combines this MOSFET with a light-emitting diode (LED) chip with high luminous efficacy and a highly sensitive photodiode array (PDA), achieving a withstand voltage of 1 500 V and low power consumption.



MCU: microcontroller unit ECU: electronic control unit IC: integrated circuit

Example of configuration of lithium-ion BMS incorporating photorelays



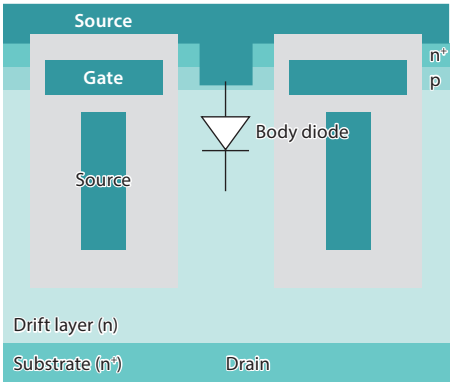
CTI: comparative tracking index

Internal structure of 1 500 V photorelay

Comparison of main characteristics of conventional and newly developed photorelays

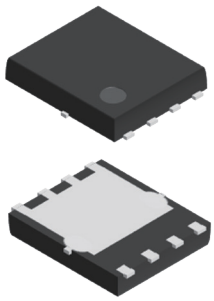
	Conventional product	New product
Part number	TLX9175J	TLX9160T
Storage temperature	-55 to 125°C	-55 to 150°C
Operating temperature	-55 to 105°C	-40 to 125°C
Insulation voltage	3 750 Vrms	5 000 Vrms
Recommended maximum operating supply voltage	450 V	1 000 V
Blocking voltage	600 V bidirectional	1 500 V bidirectional
Maximum trigger LED current	3 mA	3 mA
Maximum on-resistance	335 Ω (LED forward current: 10 mA, on current: 15 mA)	250 Ω (LED forward current: 10 mA, on current: 50 mA)

4.3 U-MOSX-H 150 V Power MOSFET



p: p-type semiconductor
n: n-type semiconductor
n^+: heavily doped n-type semiconductor

Cell structure of field-plate trench MOSFET



Outline of U-MOSX-H
(5×6 mm^2)

Comparison of main characteristics of conventional U-MOSVIII-H series and newly developed U-MOSX-H series products

Characteristic	Previous product U-MOSVIII-H	Newly developed product U-MOSX-H
V_{DSS} (V)	150	150
V_{th} (V)	2.0 to 4.0	3.3 to 4.3
T_{ch} (°C)	150	**175**
$R_{DS(ON)}$ (V_{GS}: 10 V) (mΩ)	13 (typ.)	**7.3 (typ.)**
$R_{DS(ON)}$·Q_{SW} (mΩ·nC)	107	**86**

V_{DSS}: drain-source voltage V_{th}: gate threshold voltage T_{ch}: channel temperature V_{GS}: gate-source voltage

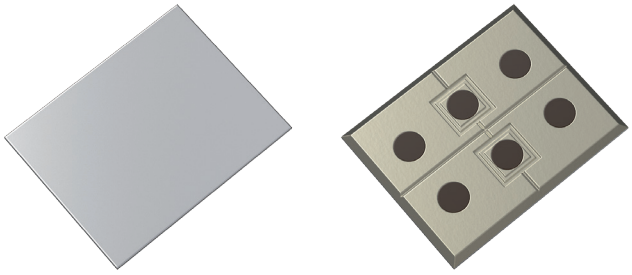
Fifth-generation (5G) mobile base stations consume considerable power because of increased communication traffic. To reduce their power consumption, it is necessary to improve the efficiency of their power supplies.

In response to this requirement, Toshiba Electronic Devices & Storage Corporation has developed the U-MOSX-H series of 150 V power MOSFETs with a significantly improved trade-off between on-resistance and gate charge.

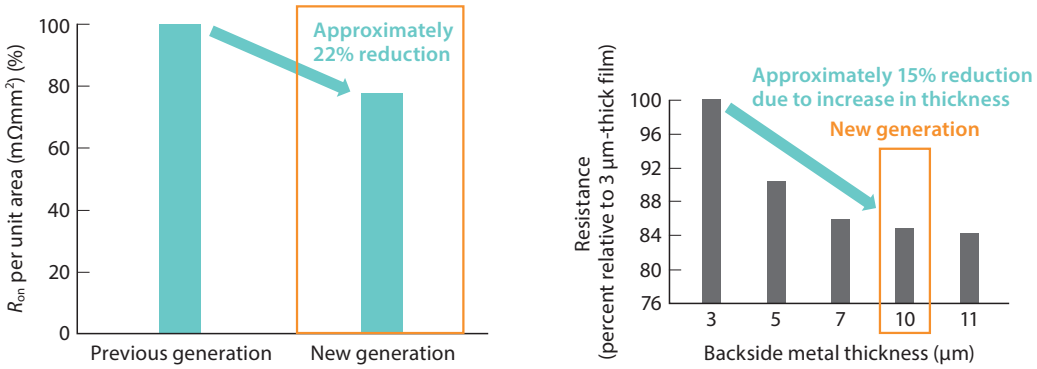
Designed based on the previous U-MOSVIII-H series, the U-MOSX-H series provides an optimized trench field-plate structure and heavily doped diffusion layers, contributing to a reduction in drain-source on-resistance ($R_{DS(ON)}$) and gate switching charge (Q_{SW}). As a result, the U-MOSX-H series provides approximately 20% lower $R_{DS(ON)}$·Q_{SW}, a key performance indicator for power efficiency, than the U-MOSVIII-H series.

At present, we are developing power MOSFETs in different packages and with different on-resistance values as well as those with a high-speed diode (HSD) offering improved body diode characteristics. These products will contribute to a further reduction in power consumption, which, in turn, will contribute to the realization of a sustainable society.

4.4 Low-Resistance Common-Drain Dual MOSFETs for Mobile Battery Protection Circuits



SSM6N951L common-drain MOSFET



Comparison of on-resistance of previous- and new-generation products

Common-drain MOSFETs are widely used in battery protection circuits for smartphones and tablets. To reduce heat dissipation during battery charging and discharging, on-resistance (R_{on}) is one of the most important characteristics required for MOSFETs.

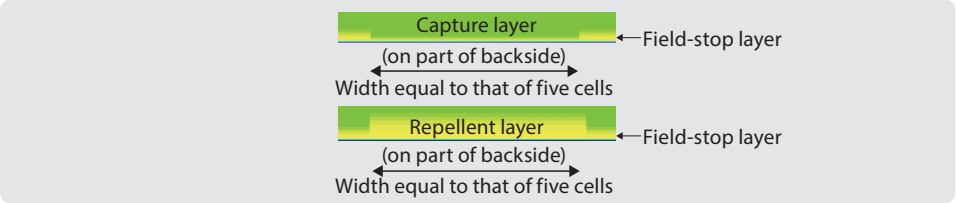
There is an ever-growing demand for MOSFETs with progressively smaller R_{on} to increase the battery capacity and reduce the charging time. In response to this trend, Toshiba Electronic Devices & Storage Corporation has developed new-generation trench-gate MOSFETs with a shrunken cell pitch (0.45 µm) that provide approximately 22% less R_{on} per unit area than the previous-generation products. Moreover, these MOSFETs are fabricated on a low-resistance silicon wafer substrate and feature a thick metal film (10 µm or more) on the side opposite to the patterned area, resulting in an approximately 15% reduction in interconnect resistance.

Drawing on these technologies, we released the SSM6N951L in 2020, followed by the SSM10N954L in 2021. These products have the same cell pitch, but the SSM10N954L provides an even more optimized device structure and substrate layer. As a result, the SSM10N954L features the industry's lowest-class R_{on} of 2.1 mΩ (at a gate-source voltage (V_{GS}) of 4.5 V)(*).

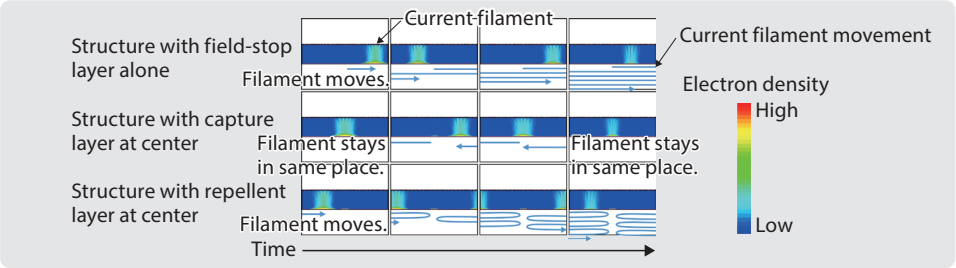
We will continue to develop MOSFET processes and products that offer even lower R_{on}.

(*) As of March 2021, in comparison with 12 V common-drain MOSFETs (as researched by Toshiba Electronic Devices & Storage Corporation)

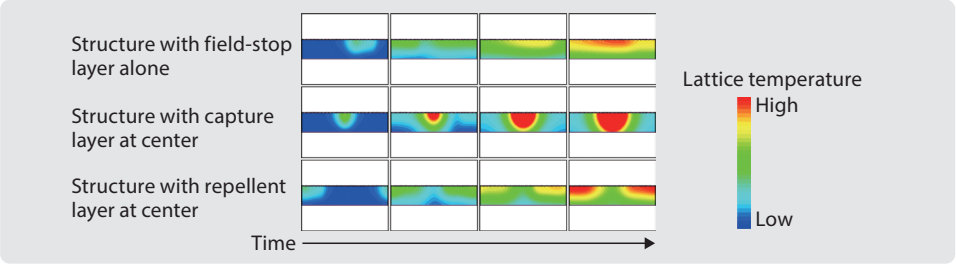
4.5 Analysis of Mechanism of Current Filament Control in IGBTs



(a) Capture and repellent layers placed in IGBT simulation structure (64 cells)



(b) Electron density distributions (64 cells)



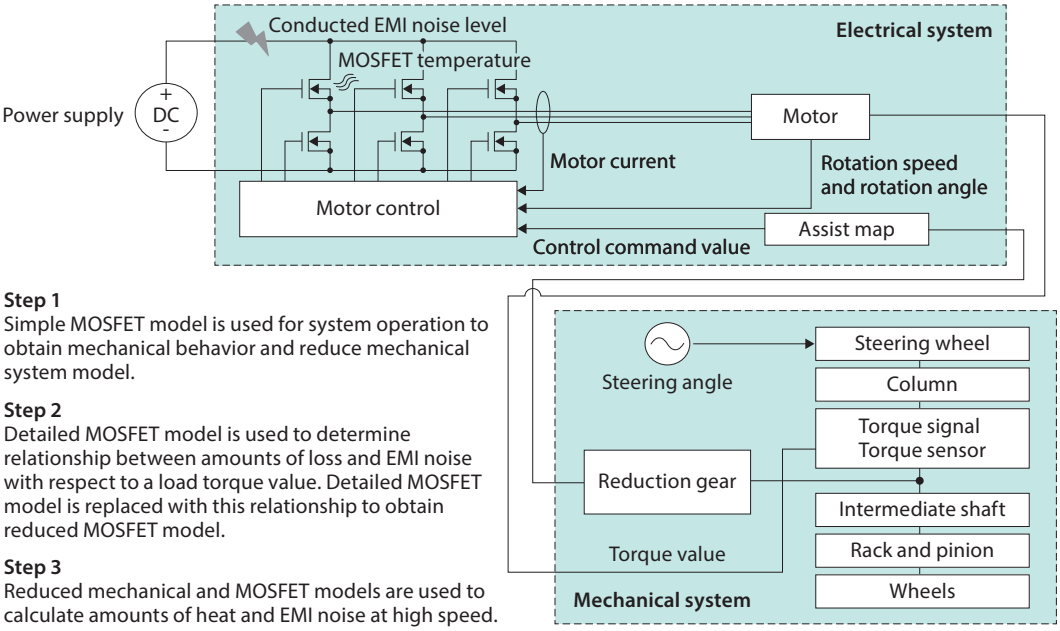
(c) Lattice temperature distributions (64 cells)

Results of simulations of current filament behavior depending on device structure of IGBTs

In recent years, there has been growing demand for improvement of the reliability of IGBTs without compromising their electrical characteristics. One of the key fundamental technologies required to improve IGBT reliability is current filament control. Current filamentation is a phenomenon in which the currents that would normally flow uniformly across a power device concentrate locally because of its inherent electronic instability. It is known that large Joule heat generated by a localized increase in current density due to current filamentation causes current filaments to move around a wide area of the device. If the movement of a current filament is stopped at a boundary or defect of the device, thermal failure might occur, significantly affecting the reliability of the device.

To solve this problem, Toshiba Electronic Devices & Storage Corporation has developed simulation environments to simulate the capture and repellent layers for controlling the movement of current filaments and analyzed their control mechanism. The capture layer captures current filaments, whereas the repellent layer repels them. From the results of this analysis, we confirmed that the relationship of the difference in local lattice temperature, the difference in the amount of carriers injected from the backside, and the temperature dependence of the negative resistance of each layer is the key to current filament control.

4.6 High-Speed, High-Accuracy Simulation Technique to Evaluate Thermal Performance and EMI Noise of Automotive Power Semiconductors for Model-Based Development



Model	Detailed model	Model reduced using Accu-ROM technique
Calculation time for EPS right turn	32 hrs. 51 min.	3 hrs. 27 min.

Calculation procedure using Accu-ROM (accurate reduced-order modeling) technique and time required for calculation of heat and EMI noise generated by electric power steering (EPS) system

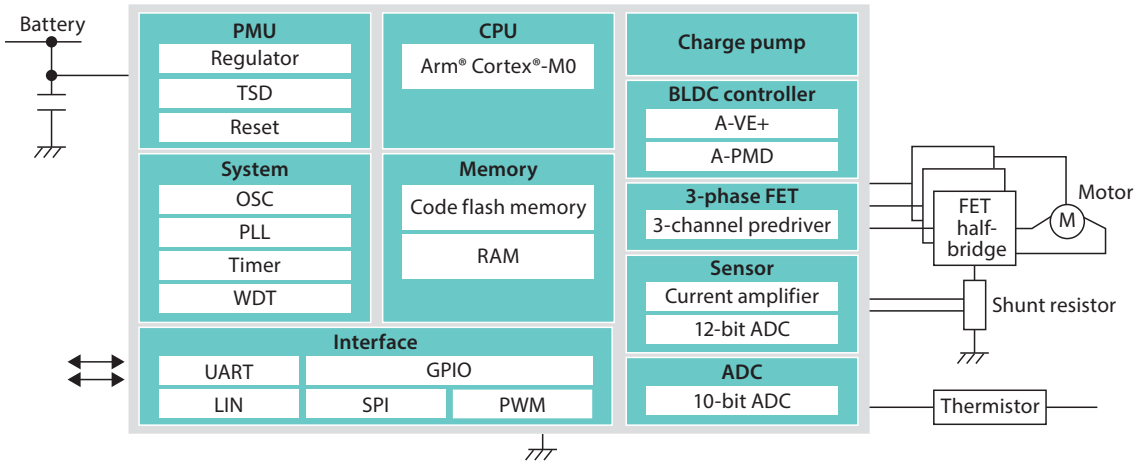
The automotive industry is introducing model-based development using simulation technology. The amounts of heat and electromagnetic interference (EMI) noise generated by automotive devices are crucial. However, since highly accurate semiconductor device models are necessary for their calculation, it has been a challenge to reduce the calculation time.

To overcome this challenge, Toshiba Electronic Devices & Storage Corporation has developed the Accu-ROM (accurate reduced-order modeling) technique, which enables accurate and fast simulations for heat and EMI noise calculation.

Specifically, the Accu-ROM technique reduces models by focusing on the differences in response time between mechanical and electrical systems. First, the behavior of the mechanical system is obtained using a simple MOSFET model, and then the mechanical model is reduced. Next, a highly accurate MOSFET model is used to determine the relationship between the amounts of heat and EMI noise with respect to a load, and the MOSFET model is replaced with this relationship to obtain a reduced MOSFET model.

The Accu-ROM technique reduces the simulation time required for heat and EMI noise calculation to roughly one-tenth of the time required by the conventional technique.

4.7 SmartMCD Integrated Motor Control Driver for Automotive Applications



PMU: power management unit
TSD: thermal shutdown
OSC: oscillator
PLL: phase-locked loop
WDT: watchdog timer
UART: universal asynchronous receiver-transmitter

GPIO: general-purpose input/output
LIN: Local Interconnect Network
SPI: Serial Peripheral Interface
PWM: pulse-width modulation
A-VE+: advanced vector engine plus
A-PMD: advanced programmable motor driver

FET: field-effect transistor
AMP: amplifier
ADC: analog-to-digital converter
BLDC: brushless DC motor
RAM: random-access memory

Architecture of SmartMCD integrated motor control driver for automotive applications

In recent years, in-vehicle electronic control unit (ECU) manufacturers have been migrating from a decentralized to a centralized zoned platform. Demand is rapidly shifting from conventional motor control driver circuits composed of many integrated circuits (ICs) such as voltage regulator, motor control driver (MCD), microcontroller unit (MCU), and communication interface ICs to integrated MCDs.

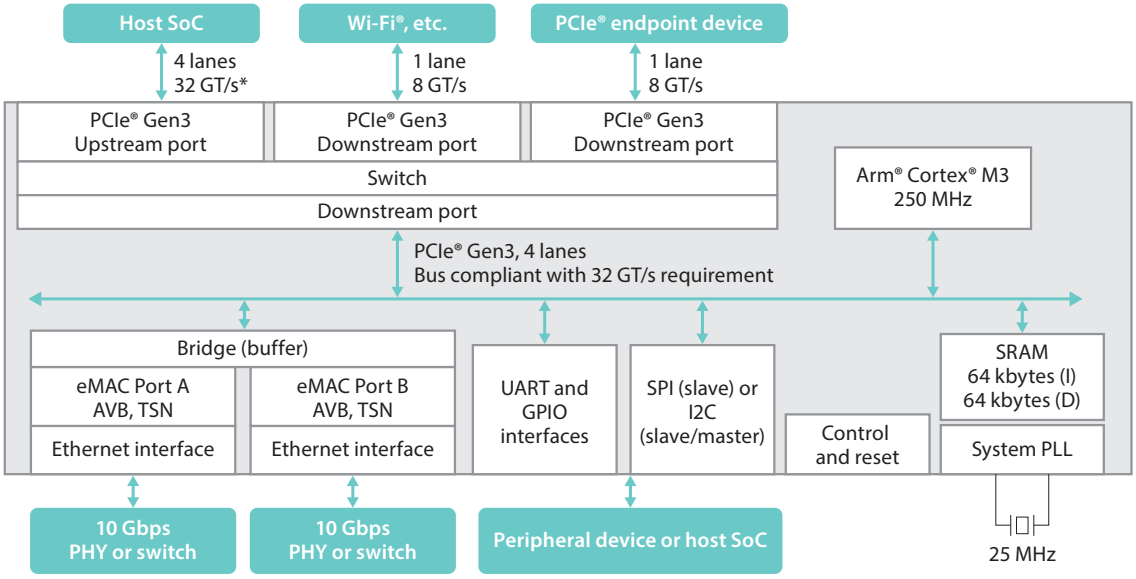
To adapt to this shift in demand, Toshiba Electronic Devices & Storage Corporation is developing the SmartMCD series of integrated MCDs for automotive applications. Fabricated with a high-voltage process, the SmartMCD series incorporates the high-performance, energy-efficient Arm® Cortex®-M0 processor, a vector engine capable of supporting various motor control applications, a programmable motor driver (PMD), a motor driver loss reduction function, and flash memory.

Housed in a small package, the SmartMCD series also provides diverse functions to support advanced motor control, including an MCU, various voltage regulators, motor predrivers, and communication interfaces. We have confirmed that, as a result of the basic design, it requires an approximately 65% smaller mounting area than a conventional motor control driver circuit composed of discrete devices.

In addition, the SmartMCD series supports model-based development using MATLAB and Simulink, which helps to shorten the time required to develop automotive embedded systems and improve the efficiency of automotive software development.

We will continue to integrate motor drivers and new functions into SmartMCD.

4.8 TC9563XBG 10 Gbps Ethernet Bridge IC for Automotive Information Communications Systems and Industrial Equipment



I2C: Inter-Integrated Circuit
SRAM: static random-access memory
PHY: physical layer
eMAC: Ethernet media access control (MAC) layer
I: instruction memory
(*) T/s: transfers per second

D: data memory
UART: universal asynchronous receiver-transmitter
GPIO: general-purpose input/output
SPI: Serial Peripheral Interface
PLL: phase-locked loop

Block diagram of TC9563XBG

Automotive networks are evolving toward zone architecture, where communications between zones use real-time, multi-gigabit transmission via Ethernet at a rate of 1 Gbps or higher.

To meet this requirement, Toshiba Electronic Devices & Storage Corporation has developed the TC9563XBG Ethernet bridge IC equipped with a 10 Gbps Ethernet interface featuring Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN) functions.

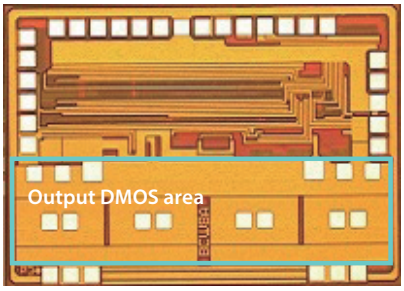
As the speeds of communications devices continue to increase, the new IC can be used not only for zone architecture but also for various automotive applications such as in-vehicle infotainment (IVI) and telematics, as well as in industrial equipment. It is also positioned to be a successor to the current TC9560 and TC9562 series products supporting 1 Gbps Ethernet.

In recent years, an increasing number of devices have been equipped with PCIe® interfaces for device-to-device communications, such as Wi-Fi®, and the host system-on-a-chip (SoC) tends to run short of PCIe® interfaces. To solve this problem, the TC9563XBG has three PCIe® Gen 3 switch ports for communications with the host SoC and connection to devices equipped with PCIe® interfaces.

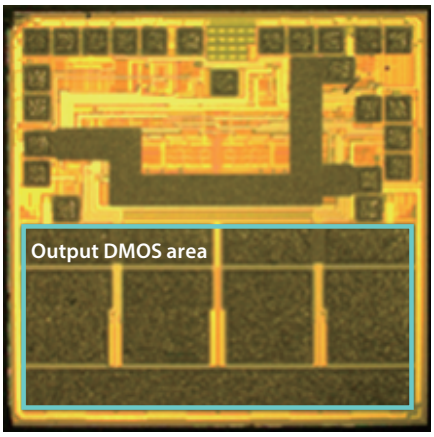
4.9 Constant-Current Stepping Motor Driver IC Fabricated Using BiCD-0.13G4 Process

Maximum ratings: 40 V, 2.0 A
Output on-resistance: 0.8 Ω
Package: WQFN48
Current-sensing resistors: Required

Maximum ratings: 40 V, 2.0 A
Output on-resistance: 0.8 Ω
Package: VQFN32
Current-sensing resistors: Not required



TB67S539FTG (fourth generation)



TB62269FTG (first generation)

Configurations of motor driver ICs fabricated using first- and fourth-generation BiCD-0.13 process technologies

Stepping motors are used in various fields, and demand for them is growing at an average annual rate of approximately 2.6%. There is a strong requirement for stepping motor driver ICs with a reduced footprint.

In response, Toshiba Electronic Devices & Storage Corporation has developed the TB67S539FTG stepping motor driver IC fabricated using the BiCD(*)-0.13G4 fourth-generation 0.13 µm analog power IC process. Leveraging the advantage of this process, the H-bridge circuit that controls the motor is composed of n-channel double-diffused MOS (DMOS) devices to achieve an on-resistance of 0.8 Ω. Furthermore, the output DMOS area of the newly developed IC is only 38% that of the conventional IC.

Housed in the 5 mm square VQFN32 package, the TB67S539FTG provides the functions required for motor control such as high-precision current control without the need for any external current-sensing resistors. In addition, the charge pump for the high-side n-channel DMOS devices of the H-bridge circuit does not require any external capacitor. Therefore, the TB67S539FTG helps to reduce both board cost and space. We commenced mass production of the TB67S539FTG in August 2021.

(*) A process for integrating bipolar, complementary MOS (CMOS), and DMOS devices on the same chip

4.10 MBM™-2000 Mask Writer Using Multiple Electron Beams

MBM™-2000 mask writer using multiple electron beams

Mask writers are key equipment for writing photomasks that are used in the lithography process for the manufacture of semiconductor devices. Mask writers using multiple electron beams, or multi-beam mask writers, offer higher speed and beam placement accuracy than conventional single-beam mask writers.

NuFlare Technology, Inc., a subsidiary of Toshiba Electronic Devices & Storage Corporation, has developed the MBM™-2000, a multi-beam mask writer capable of writing extreme ultraviolet (EUV) and complex photomasks for 3 nm-generation semiconductor devices and shipped the first unit in April 2021.

The MBM™-2000 incorporates a newly developed device capable of rapidly and independently controlling about 260 000 electron beams. It has achieved a critical dimension precision of 0.7 nm (3σ) and an image placement precision of 1.4 nm (3σ). This device was jointly developed by the Corporate Research & Development Center of Toshiba Corporation and Toshiba Electronic Devices & Storage Corporation. In addition, pixel-level dose correction (PLDC) can control the electron beam exposure of each pixel 16 nm square in 64 increments, enabling high-accuracy patterning. Furthermore, the dedicated MBM™ data format (MBF) helps to minimize the increase in data volume even for complex patterns.

4.11 EPIREVO™ S8 Single-Wafer SiC Epitaxial Reactor

EPIREVO™ S8 single-wafer epitaxial reactor for SiC power devices

To date, NuFlare Technology, Inc. has commercialized two single-wafer epitaxial growth reactors for power semiconductor devices: the EPIREVO™ S6 for 150 mm SiC wafers and the EPIREVO™ G8 for 200 mm gallium-nitride (GaN) wafers. In response to the trend toward increasing wafer diameter in the SiC market, we have now developed the EPIREVO™ S8, which supports SiC wafers with a diameter of 200 mm.

While inheriting the basic design of the EPIREVO™ S6, which applies high-speed wafer rotation technology to vertical chemical vapor deposition (CVD), the EPIREVO™ S8 has redesigned gas inlet and heater structures to enable uniform deposition across a large-diameter wafer.

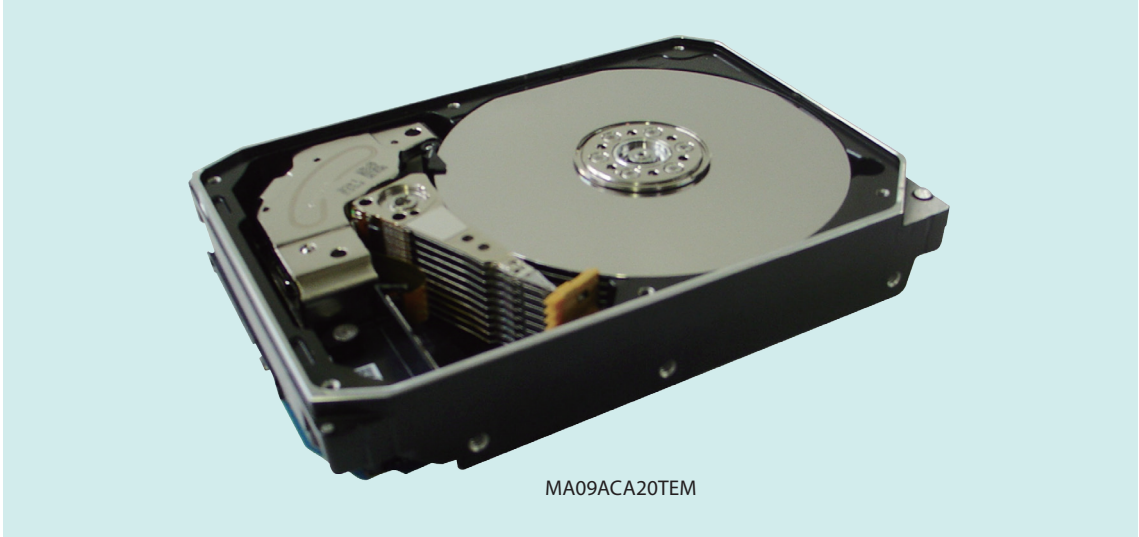
The basic specifications of the EPIREVO™ S8 are as follows:

- Maximum growth temperature: 1 650°C
- Temperature uniformity: ±5°C
- Maximum wafer rotation speed: 1 000 rpm
- Controlled pressure range: 2.0 to 93.3 kPa.

An evaluation using 150 mm wafers showed a growth rate of 54 µm/h, a thickness uniformity of within ±1.5%, and a doping uniformity of within ±3.7%, which are equivalent to those of the EPIREVO™ S6.

Our next step is to develop processes for 200 mm wafers to achieve high-speed growth, high uniformity, and low defect density.

4.12 MA09 Series 3.5-Inch HDDs for Data Centers with Maximum Storage Capacity of 20 Tbytes Applying FC-MAMR and SMR Technologies



20 Tbyte 3.5-inch SMR HDD for data centers

In the face of the ever-accelerating development of a data-driven society, it is becoming increasingly important to develop solutions for storing huge volumes of electronic data for data centers.

Under these circumstances, Toshiba Electronic Devices & Storage Corporation has released the MA09 series of 3.5-inch shingled magnetic recording hard disk drives (SMR HDDs) for data centers with the industry's largest capacity of 20 Tbytes(*1). The MA09 series is designed based on the MG09 series, the industry's first HDD series applying flux-control microwave-assisted magnetic recording (FC-MAMR) technology(*1).

The MA09 series provides two features: (1) enhanced redundant sector processing, a technology having a high affinity with SMR, to improve data reliability and (2) servo control with improved accuracy of head position prediction to suppress write performance degradation while securing data quality.

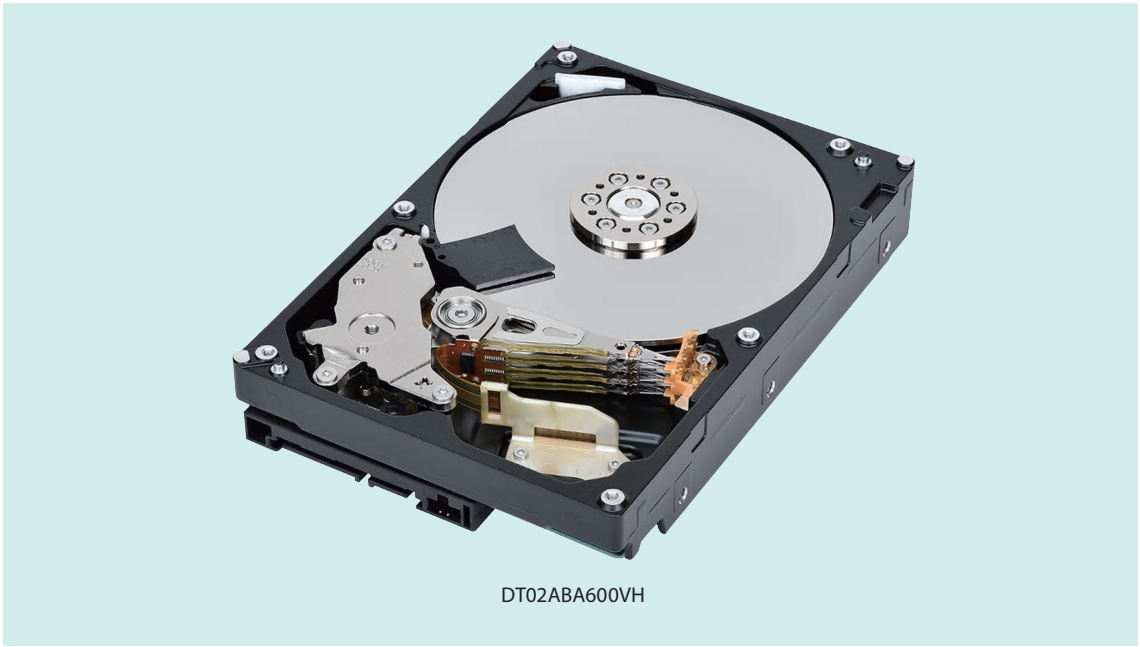
In order to capitalize on the advantage of SMR in increasing the track density(*2), we have maximized the areal recording density of the MA09 series by reducing the linear recording density(*3) by roughly 6% and increasing the track density by roughly 23% in comparison with the MG09 series. As a result, the MA09 series provides approximately 11% higher storage capacity than the MG09 series.

(*1) As of July 2021 for 3.5-inch HDDs with a height of 26.1 mm (as researched by Toshiba Electronic Devices & Storage Corporation)

(*2) Track density: Recording density in the cross-track direction (i.e., radial direction on the platter)

(*3) Linear recording density: Recording density in the down-track direction (i.e., circumferential direction on the platter)

4.13 3.5-Inch Large-Capacity, High-Performance Surveillance HDDs Applying SMR Technology



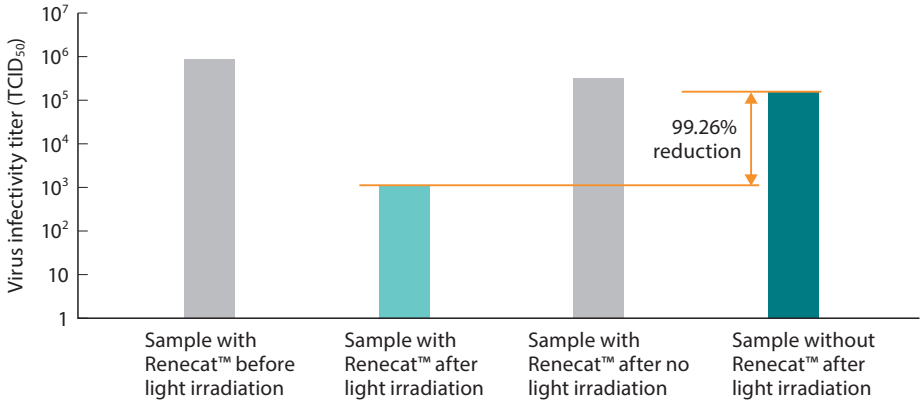
6 Tbyte 3.5-inch SMR HDD for surveillance camera systems

Accompanying the expansion of the surveillance camera market, the demand for large-capacity, high-performance HDDs for surveillance digital video recorders and surveillance network video recorders is growing.

To meet this demand, Toshiba Electronic Devices & Storage Corporation has released the DT02-VH series of 3.5-inch surveillance HDDs with a storage capacity of 2 Tbytes per platter. The DT02-VH series uses SMR to increase the recording density while incorporating firmware optimized for multi-stream surveillance environments to deliver high performance.

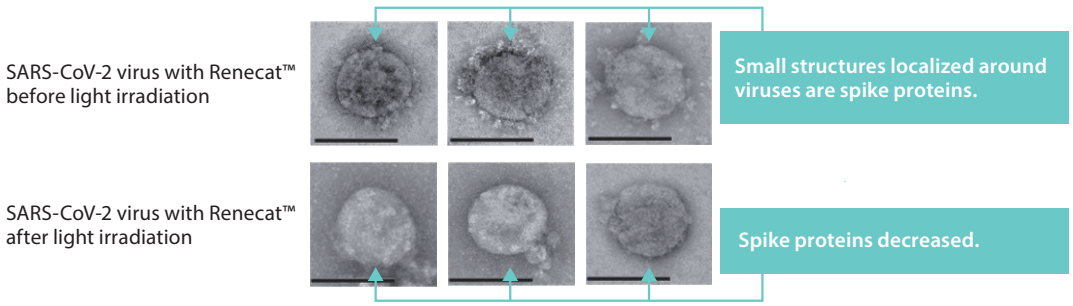
In order to efficiently record multiple streams of video data from many cameras simultaneously, we optimized the recording process to directly write to the SMR area without going through a media cache (MC). The DT02-VH series also provides a conventional magnetic recording (CMR) area for the recording of system data that is small in size. As a result, the DT02-VH series has sufficient performance to allow up to 64 cameras to be connected.

4.14 Antiviral Effect of Renecat™ Photocatalyst against Novel Coronavirus (SARS-CoV-2)



* Test conditions: 30 × 30 mm sheet glass coated with 4 g of Renecat™ per m^2. Antiviral activity tests using the film adhesion method with reference to the International Organization for Standardization (ISO) 18071:2016 standard.

$TCID_{50}$: 50% tissue culture infectious dose (the dilution of a virus required to infect 50% of a given tissue culture)



* Based on Uema, M. et al. 2021. *Biocontrol Science* 26(2):119–125.

Results of verification tests on effectiveness of Renecat™ photocatalyst for suppression of COVID-19 infection

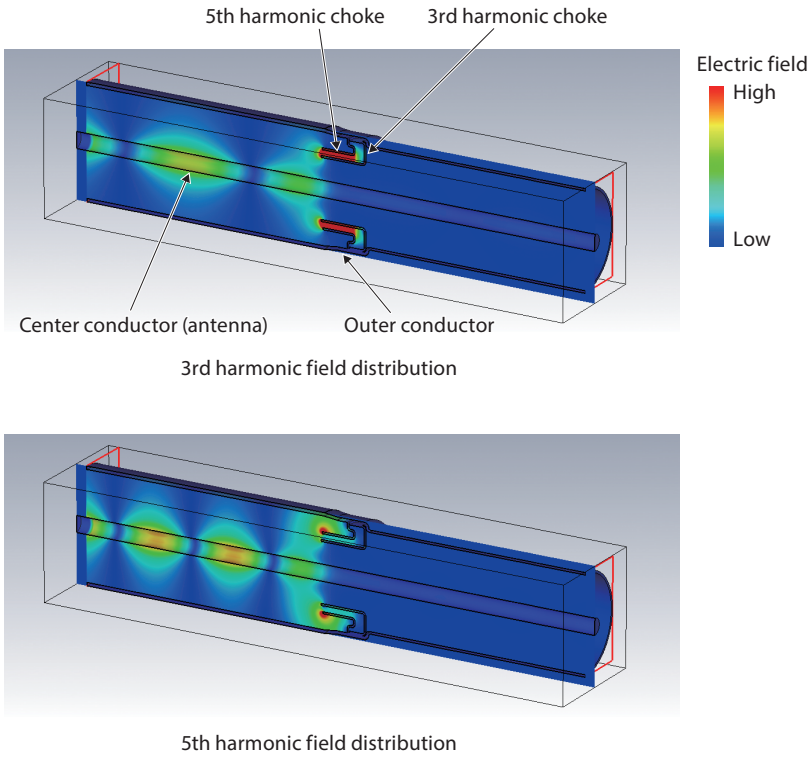
Renecat™ is a photocatalyst that exhibits antibacterial, antiviral, and deodorant effects under visible light irradiation. Toshiba Materials Co., Ltd. has confirmed the antiviral effects of Renecat™ against the influenza A virus and other viruses in the past.

We have now examined its antiviral effect against the novel coronavirus (SARS-CoV-2) as one of the research themes of the "Study on the control of a novel coronavirus (2019-nCoV)" project funded by the Japan Agency for Medical Research and Development (AMED).

The results of this research revealed that samples of sheet glass with Renecat™ showed a more than 99.2% reduction in virus infectivity titer after six hours of 3 000 lx fluorescent light irradiation at 20°C (with ultraviolet light cut off by a filter) compared with those without Renecat™.

Furthermore, scanning electron microscope (SEM) imaging and immunoblot analysis of the virus after light irradiation confirmed that spike proteins, which are the parts of the novel coronavirus that bind to human cells, decreased as a result of Renecat™ coating. These results suggest that Renecat™ acts on the novel coronavirus under visible light.

4.15 Magnetron Noise Suppression Using Optimally Designed Harmonic Filter Choke



Result of simulation using optimization tool at harmonic suppression choke structure design stage

A magnetron is used as the microwave source in microwave ovens. To reduce the noise generated in the magnetron, it is necessary to optimize the shapes of the harmonic filter chokes in the output section. Conventionally, simulation, prototyping, and verification were repeated to fine-tune the inside and outside diameters and lengths of the chokes as well as their combinations according to the frequency band to be suppressed.

Toshiba Hokuto Electronics Corporation has now introduced integrated simulator software and its optimization tool. We created a complicated simulation model incorporating choke length and other design parameters based on the three-dimensional (3D) data of the output section. Using this model, we performed simulations while changing the design parameters until the propagation of the third and fifth harmonics was minimalized, and obtained design dimensions close to the dimensions of pressed components.

As a result of prototyping and verification, we succeeded in reducing the magnitudes of the third and fifth harmonics by about 8 dB and 11 dB, respectively. In addition, the improved simulation accuracy helped to reduce the number of iterations of prototyping and verification.

We will use this simulator not only to design the output section of magnetrons but also to improve other products and customer services.