TOSHIBA

UM-TS03***-E018

PROGRAMMABLE CONTROLLER PROSEC T3

PULSE INPUT MODULE PI312 USER'S MANUAL

TOSHIBA CORPORATION

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Safety Precautions

This module (PI312) is a pulse input module for Toshiba's Programmable Controller PROSEC-T3 (hereafter called T3). Read this manual thoroughly before using this module. Also, keep this manual and related manuals so that you can read them anytime while this module is in operation.

Safety Symbols

The following safety symbols are used on the product and/or in the related manuals. Pay attention to information preceded by the following symbols for safety.

- WARNING Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION** Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury. It may also be used to alert against unsafe practices.

Safety Precautions

- Turn off power to the T3 and to the PI312 before removing or mounting the PI312. Failure to do so can cause electrical shock or damage to this product.
- Read the Safety Precautions described in the T3 User's Manual before using the T3 and the PI312.
- Follow the instructions described in this manual and in the T3 User's Manual when installing and wiring the T3 and the PI312.
- The PI312 has been designed for the T3. Use your PI312 only on the rack of the T3.
- Remove the PI312 from the rack before setting the jumper plugs on the PI312. Do not touch other components on the PI312's printed circuit board. It may cause damage to the PI312.
- The PI312 consumes maximum 0.8 A of internal 5 Vdc power. Confirm that the total 5 Vdc consumed current per one power supply module is within the limit (7A). If it exceeds the limit, the T3 cannot operate properly and this may cause unsafe situation.

About This Manual

About This Manual

This manual explains the specifications and operations of the Pulse Input Module (PI312) for Programmable Controller T3. Read this manual carefully before using the PI312.

Inside This Manual

Section 1 Overview

This section introduces the PI312. The PI312 has nine (9) operation modes. This section outlines the PI312's operation modes. Read this section at first to get basic understanding of the operation modes and to decide the operation mode for your intended application. The external features of the PI312 are also provided in this section.

Section 2 Specifications

This section provides the hardware and functional specifications of the PI312. Refer to this section to check applicability of the PI312 with your intended system.

Section 3 Wiring

This section provides the information for external wire connections. Depending on the operation modes, wire connections are different. Read this section after you have decided the operation mode. Wiring precautions are also provided in this section.

Section 4 Register Configuration

This section provides the information to design T3 program for the PI312. This section explains the I/O allocation and functions of the I/O registers assigned to the PI312. Also, this section explains the buffer memory contents which is provided in the PI312, and how to access the buffer memory by T3 program.

Section 5 Operation Mode Setting

This section explains the method for setting the PI312 to your desired operation mode. The PI312's operation mode is determined by setting the jumper plugs on the PI312 and by writing a mode data into the PI312's buffer memory. T3 sample programs for setting the PI312's operation mode are provided in this section.

Section 6 Function Details

This section explains details of each operation mode. This section consists in nine (9) clauses according to the operation modes. Each clause contains the explanation for functions, necessary external signals, I/O register and buffer memory usage, and T3 sample programs. Read the clause for your intended operation mode.

Section 7 Interrupt Function

The PI312 can generate interrupt signal for T3. This section provides the information to design the T3 interrupt program. The interrupt generation timing is explained in section 6.

Appendix

The specifications of READ and WRITE instructions are described. These instructions are used for interchanging data between T3 and PI312.

2 Pulse Input Module (PI312)

Related Manuals

The following related manuals are available for T3. Besides this manual, read the following manuals for your better understanding.

T3 User's Manual - Hardware

This manual covers the T3's main body and basic I/O - their specifications, handling, maintenance and services.

T3 User's Manual - Functions

This manual explains the functions of the T3 and how to use them. The necessary information to create user program is covered in this manual.

T-series Instruction Set

This manual provides the detailed specifications of instructions for Toshiba's T-series Programmable Controllers.

T-series Computer Link Function

This manual provides the information for a computer to communicate with T3 through the T-series Programmable Controller's Computer Link function.

T-PDS (Ver. 1.4) Basic Operation manual

This manual explains how to install the T-series program development system (T-PDS) into your computer and provides basic programming operations.

T-PDS (Ver. 1.4) Command Reference Manual

This manual explains the T-series program development system (T-PDS) in detail.

T-PDS (Ver. 1.6) Expanded Functions

This manual explains the expanded functions on the T-PDS version 1.6. This manual supplements the T-PDS (Ver.1.4) Command Reference Manual.

T-series Handy Programmer (HP911) Operation Manual

This manual explains the functions and key operations of the T-series Handy Programmer (HP911).



Other than the listed above, some T3 related manuals for special I/O modules and data transmission modules are available. Contact Toshiba for more information.

Contents

Contents

| Safety | Precautions | 1 |
|---------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| About 1 | This Manual | 2 |
| 1. | PI312 Overview | 7 |
| 1.1 1.2 1.2.1 1.2.2 1.3 | Introduction Operation mode overview Counter operation mode Pulse count mode External features | 8 9 9 17 18 |
| 2. | Specifications | 21 |
| 2.1 2.2 2.3 2.4 | General specifications Functional specifications Input/output specifications Input/output internal circuit | 22 22 23 24 |
| 3. | Wiring | 27 |
| 3.1 3.2 3.3 | Terminal arrangement Signal connections Wiring precautions | 28 29 32 |
| 4. | Register Configuration | 33 |
| 4.1 4.2 4.2.1 4.2.2 4.2.3 4.2.4 4.2.5 4.2.6 4.2.7 | I/O allocation and I/O registers PI312 buffer memory Memory map Buffer memory access Count value registers Upper and lower comparison value registers Hold value registers Interrupt flags Operation mode registers | 34 36 37 39 40 41 42 43 |
| 5. | Operation Mode Setting | 45 |
| 5.1 5.2 5.3 | Mode setting overview Jumper plug setting Operation mode register setting | 46 47 48 |

Contents

| 6. | Function Details | 51 |
|------------|---------------------------------------|----------|
| 6.1 | Quadrature bi-pulse counter mode | 52 |
| 6.2 | Up/down pulse counter mode | 56 |
| 6.3 | Auto-reset universal counter mode | 60 |
| 6.4 | Universal counter mode | 64 |
| 6.5 | Speed counter mode | 68 |
| 6.6 | Programmable interval timer mode | 72 |
| 6.7 | Gate-ON timer mode | 76 |
| 6.8 | Slave counter mode | 80 |
| 6.9 | Slave timer mode | 85 |
| 7. | Interrupt Function | 91 |
| 7.1 | Interrupt function | 92 |
| 7.2 | Interrupt control flags | 92 |
| 7.3 | T3 sample program | 93 |
| 7.4 | Precautions on interrupt function | 94 |
| Appen | dix | 95 |
| | | |
| A.1 | Specification of the READ instruction | 96 |
| A.1 A.2 | Specification of the READ instruction | 96 98 |

Section 1

PI312 Overview

1.1 Introduction

1.2 Operation mode overview

1.3 External features

1.1 Introduction

The pulse input module PI312 (hereafter called PI312) is a high-speed pulse counter module for Toshiba's Programmable Controller PROSEC-T3 (hereafter called T3). The PI312 has 2 channels of pulse inputs, channel 1 (CH1) and channel 2 (CH2), and can count up to 50 kHz (pulses per second) pulses individually for each channel.

The pulse input voltage can be selected either 5 Vdc or 12 Vdc by selecting the connection terminals.

The PI312 has total 9 operation modes as listed below.

- (1) Quadrature bi-pulse counter mode
- (2) Up/down pulse counter mode
- (3) Auto-reset universal counter mode
- (4) Universal counter mode
- (5) Speed counter mode
- (6) Programmable interval timer mode
- (7) Gate-ON timer mode
- (8) Slave counter mode
- (9) Slave timer mode

In the above (1) through (5) modes, the PI312 counts external pulses. In the (6) and (7) modes, the PI312 counts its internal clock pulses, resulting it functions as timer. These (1) through (7) modes can be set individually for channel 1 and channel 2. In the (8) and (9) modes, PI312's two channels work relatively.

The operation mode of the PI312 can be set by user. Refer to section 5. The function of each operation mode is outlined in section 1.2, and explained in detail in section 6.

The PI312 can be applied for wide range of applications by selecting the operation mode.



- (1) Correct setting of the operation mode is important to use the PI312. If it has not set correctly, the PI312 will not work as expected.
 - (2) The maximum number of PI312s that can be controlled by one T3 is not limited by software. However, the PI312 consumes maximum 0.8 A of internal 5 Vdc power. Confirm that the total 5 Vdc consumed current per one power supply module is within the limit (7 A). Refer to the T3 User's Manual Hardware.

1.2 Operation mode overview

This section outlines the PI312's operation modes. Read this section to get basic understanding of the operation modes.

1.2.1 Counter operation mode

(1) Quadrature bi-pulse counter mode

PI312 counts the pulses whose phases are shifted 90° each other. When phase A pulse precedes against phase B pulse, the PI312 counts up (increase). On the other hand, when phase B pulse precedes, the PI312 counts down (decrease).

When the count value is increased by 1 in the upper limit value (16777215), it is reset to 0 (zero). When the count value is decreased by 1 in the lower limit value (0), it is reset to the upper limit value (16777215).

2 points of comparison values can be set. These are called set-point-1 and set-point-2. When the count value is greater than the set-point-1, the PI312's hardware comparison output (*S1) comes ON. When the count value is smaller than the set-point-2, the PI312's hardware comparison output (*S2) comes ON.

Note) The asterisk (*) in the above paragraph represents 1 or 2. 1S1 and 1S2 are the outputs for channel 1, and 2S1 and 2S2 are the outputs for channel 2.

The count value is stored in the PI312's buffer memory. This value can be read or written (preset) by T3 with the READ instruction (FUN237) or the WRITE instruction (FUN238), as well as the set-point-1 and set-point-2.

The interrupt function can also be used. When the count value reaches the set-point-1 in counting up or it reaches the set-point-2 in counting down, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately.



Pulse form (time chart)



(2) Up/down pulse counter mode

PI312 counts up (increase) by the pulses into phase A, and counts down (decrease) by the pulses into phase B.



All other functions are the same as that of (1) Quadrature bi-pulse counter mode.

(3) Auto-reset universal counter mode

PI312 counts up by the single phase pulses into phase A. When the count value reaches the set-point-1, the count value is reset to 0 (zero). And at the same time, the PI312 generates interrupt signal for the T3. The set-point-1 can be set in the range of 1 to 16777215.



(4) Universal counter mode

PI312 counts up by the single phase pulses into phase A.

Different from the (3) Auto-reset universal counter mode, the counting continues until the upper limit value (16777215). When the count value exceeds the upper limit value, it is reset to 0 (zero).

PI312's comparison output for the set-point-1 (*S1) can be used.



(5) Speed counter mode

PI312 counts the single phase pulses into phase A during the specified sampling time. Then the PI312 transfers the count value in a sampling time into the hold register which is allocated on the PI312's buffer memory.

By using this mode, the frequency of the pulses can be measured.

The sampling time can be selected from 0.01 second or 0.1 second. When the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. PI312's comparison output for the set-point-1 (*S1) can be used.



 ΔT : sampling time = 0.01s or 0.1s

(6) Programmable interval timer mode

Instead of external pulses, PI312 counts its internal clock pulses. The frequency of the internal clock can be selected from 1, 10 or 100 kHz. All other functions are the same as that of (3) Auto-reset universal counter mode.

By using this mode, the PI312 can be used as a cyclic interrupt generator for the T3.



(7) Gate-ON timer mode

PI312 functions to measure the ON duration of the external pulses into phase G. The time is measured by PI312's internal clock. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

When the phase G signal is changed form OFF to ON, the PI312 resets the counter value. Then when the signal is changed from ON to OFF, the PI312 transfers the count value into the hold register which is allocated on the PI312's buffer memory.

When the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. PI312's comparison output for the set-point-1 (*S1) can be used.



(8) Slave counter mode

In this mode, the channel 2 works relatively with the channel 1 operation. The channel 1 is set as (3) Auto-reset universal counter mode. The channel 2 counts the single phase pulses into phase A in the interval of the channel 1 interrupt generation. The channel 2 count value in the interval is transferred into the channel 2 hold register. When the channel 2 count value reaches the channel 2's set-point-1, the PI312

When the channel 2 count value reaches the channel 2's set-point-1, the PI312 generates interrupt signal for the T3.

This mode is usable when two pulses are used relatively.



(9) Slave timer mode

In this mode, the channel 2 works relatively with the channel 1 operation. The channel 1 is set as (3) Auto-reset universal counter mode. Different from the (8) Slave counter mode, the channel 2 counts the internal clock pulses in the interval of the channel 1 interrupt generation. The frequency of the internal clock can be selected from 1, 10 or 100 kHz. All other functions are the same as that of (8) Slave counter mode.

This mode is usable to measure the frequency of external pulses.



1.2.2 Pulse count mode

The PI312 has 2 modes for pulse counting. They are the normal count mode and the precision count mode.

In the normal count mode, the PI312 counts at either rising or falling edge of the pulse. On the other hand, in the precision count mode, the PI312 counts at both rising and falling edges. See the timing diagram below.

The pulse count mode can be selected individually for channel 1 and channel 2.

Quadrature bi-pulse counter mode:



<Precision count mode>



1.3 External features



Status LEDs

Indicates the PI312 operation status. 6 LEDs are provided for each channel.

| А | Lit when the phase A pulse input is ON (see Note 1) |
|-----|------------------------------------------------------------------------|
| В | Lit when the phase B pulse input is ON |
| EXT | Lit when the external limit input (EXT) is ON |
| S1 | Lit when the comparison output (*S1) is ON |
| S2 | Lit when the comparison output (*S2) is ON |
| G | Lit when both the phase G (gate) and the soft-gate are ON (see Note 2) |



- (1) In the programmable interval timer mode, this LED is controlled by the internal clock.
- (2) For the soft-gate, refer to section 4.1.

Channel 1 and Channel 2 pulse input terminals

Used to connect the external pulse input signals. 16 terminals are provided for each channel.

| Terminal No. Signal | | Signal | I Description | |
|---------------------|-----|--------|------------------------------------------------------|----------------------|
| CH1 | CH2 | name | | |
| 1 | 17 | A12 | 0 V terminal for 12 Vdc input | |
| 2 | 18 | AP | Plus voltage terminal, 12 or 5 Vdc | Phase A input |
| 3 | 19 | A5I | 0 V terminal for 5 Vdc input | |
| 4 | 20 | BP | Plus voltage terminal, 12 or 5 Vdc | |
| 5 | 21 | B12 | 0 V terminal for 12 Vdc input | Phase B input |
| 6 | 22 | B5 | 0 V terminal for 5 Vdc input | |
| 7 | 23 | G12 | 0 V terminal for 12 Vdc input | |
| 8 | 24 | GP | lus voltage terminal, 12 or 5 Vdc Phase G (gate) inp | |
| 9 | 25 | G5I |) V terminal for 5 Vdc input | |
| 10 | 26 | MP | Plus voltage terminal, 12 or 5 Vdc Phase M (mark) | |
| 11 | 27 | M12 | V terminal for 12 Vdc input input | |
| 12 | 28 | M5 | 0 V terminal for 5 Vdc input | |
| 13 | 29 | -EXT | 0 V terminal | External limit (EXT) |
| 14 | 30 | +EXT | Plus voltage terminal, 12 or 24 Vdc | input |
| 15 | 31 | SP | No use | |
| 16 | 32 | SHIELD | Cable shield connection terminal | |
| | | | (internally connected to the T3's frame ground) | |



- (1) Internal circuit for each phase input or EXT input is isolated each other.
- (2) For external wiring, refer to section 3.

Hardware comparison output terminals

Used for PI312's hardware comparison output function.

| Terminal | Signal | Description | |
|----------|-----------|-----------------------------------------------------------|---------------|
| No. | name | | |
| 33 | 1S1 | ON when count value > set-point-1 | For channel 1 |
| 34 | 1S2 | ON when count value < set-point-2 | |
| 35 | 2S1 | ON when count value > set-point-1 | For channel 2 |
| 36 | 2S2 | ON when count value < set-point-2 | |
| 37 | 24Vdc (+) | 24 Vdc terminal for the hardware comparison outputs | |
| 38 | 24Vdc (-) | 0 V (common) terminal for the hardware comparison outputs | |



- (1) The hardware comparison output function is enabled when the output-enable flag is set to ON. Refer to section 4.1 for the output-enable flag.
- (2) For external wiring, refer to section 3.

Jumper plugs

2 jumper plugs are provided on the PI312's printed circuit board. Use tweezers to change the settings.



Section 2

Specifications

- 2.1 General specifications
- 2.2 Functional specifications
- 2.3 Input/output specifications
- 2.4 Input/output internal circuit

2. Specifications

2.1 General specifications

| Item | Specifications | Remarks |
|--------------------------|--------------------------------------|----------|
| Power voltage | 5 Vdc (supplied from back plane bus) | |
| Current consumption | 0.8 A (5 Vdc) maximum | Note (1) |
| Environmental conditions | Conforms to T3 specifications | |
| Insulation resistance | 10 MΩ (1000 Vdc) | Note (2) |
| Withstand voltage | 1500 Vac - 1 minute | Note (2) |
| Size | T3 I/O module size (1 slot) | |
| Weight | 500 g | |

- Note (1) The T3's power supply module can supply maximum 7 A of internal 5 Vdc. Check that the internal 5 Vdc current consumption per one power supply module does not exceed the limit.
- Note (2) Between external terminals and internal circuit.

2.2 Functional specifications

| Item | Specifications | |
|------------------------|--------------------------------------------------|--|
| Module type | Pulse input | |
| I/O allocation type | iX+Y 2W | |
| Number of pulse input | 2 channels | |
| channels | | |
| Counter configuration | 24-bit, binary counter | |
| | Count value = 0 to 16777215 | |
| Input pulse frequency | 50 kHz maximum | |
| Counter operation mode | Quadrature bi-pulse counter | |
| | Up/down pulse counter | |
| | Auto-reset universal counter | |
| | Universal counter | |
| | Speed counter | |
| | Programmable interval timer | |
| | Gate-ON timer | |
| | Slave counter | |
| | Slave timer | |
| Pulse count mode | Normal mode (1 count per 1 pulse) | |
| | Precision count mode (both rising and falling | |
| | edges) | |
| Interrupt function | Interrupt generation for T3 at; | |
| | Count value = set-point-1 (counting up) | |
| | Count value = set-point-2 (counting down) | |
| Hardware comparison | 2 points for each channel (transistor outputs) | |
| output function | *S1: ON when Count value > set-point-1 | |
| | *S2: ON when Count value < set-point-2 | |

2.3 Input/output specifications

• Input

| Item | | Specifications | |
|---------|---------------------|--------------------------------------------------------|--|
| Phase A | Input voltage | 12 Vdc \pm 5% or 5 Vdc \pm 5% (terminal selection) | |
| Phase B | Input current | 16 mA | |
| Phase G | Minimum ON voltage | 9 V (12 Vdc input) or 3.75 V (5 Vdc input) | |
| Phase M | Maximum OFF voltage | 3 V (12 Vdc input) or 1.25 V (5 Vdc input) | |
| | Pulse duration | 10 µs or more (ON level/OFF level) | |
| | ON/OFF transition | 3 μs or less | |
| EXT | Input voltage | 12 - 24 Vdc +10%/-15% | |
| | Input current | 10 mA (24 Vdc) | |
| | Minimum ON voltage | 9.6 V | |
| | Maximum OFF voltage | 3.5 V | |

• Output

| Item | | Specifications | |
|-------------|----------------|-------------------------------------|--|
| 1S1, 1S2 | Output method | Transistor output (current sinking) | |
| 2S1, 2S2 | Output voltage | 12 - 24 Vdc | |
| | Output current | 100 mA or less (24 Vdc) | |

2. Specifications

2.4 Input/output internal circuit

• Pulse input circuit (phase A/B/G/M)



• External limit input (EXT)





• Hardware comparison output circuit (1S1, 1S2, 2S1 and 2S2)

Section 3

Wiring

- 3.1 Terminal arrangement
- 3.2 Signal connections
- 3.3 Wiring precautions

3. Wiring

3.1 Terminal arrangement

The following figure shows the terminal arrangement of the PI312's external signal connection terminal block.



PI312 terminal block

3.2 Signal connections

• Pulse input signals

Either 12 Vdc or 5 Vdc can be used for the signal voltage. For 12 Vdc, terminals P and 12 are used. (represents A, B, G or M) For 5 Vdc, terminals P and 5 (or 5I) are used. When the voltage is applied between P and 12 or between P and 5 (or 5I), the PI312 recognizes the signal is ON. The figure below shows the typical connections for a channel.

In case of 12 Vdc input system:



3. Wiring

In case of 5 Vdc input system:



• Hardware comparison output signals

2 points of hardware comparison output are provided for each channel. 1S1 and 1S2 are for channel 1, and 2S1 and 2S2 are for channel 2. The output method is 24 Vdc transistor output (current sinking). The figure below shows the typical wiring connections.





- (1) The hardware comparison output function is enabled when the output-enable flag is set to ON. Refer to section 4.1 for the output-enable flag.
- (2) The 24 Vdc power is not required if the hardware comparison outputs are not used.

3. Wiring

3.3 Wiring precautions

Turn off power to the T3 and to the PI312 before wiring. Failure to do so can cause electrical shock or damage to the PI312.

- Use shielded twisted-pair cable for the pulse input signals to minimize interference of noise.
- Normally connect the cable shield to the PI312's SHIELD terminal. This terminal is internally connected with the T3's frame ground. However if this connection results in multi-point grounding, disconnect the cable shield from the SHIELD terminal and keep single-point grounding.
- The required signals are dependent on the PI312's operation mode. Check your operation mode for the necessary signals.

Section 4

Register Configuration

4.1 I/O allocation and I/O registers4.2 PI312 buffer memory

4. Register Configuration

4.1 I/O allocation and I/O registers

The PI312 has the I/O type 'i X+Y 2W' for I/O allocation. When the automatic I/O allocation is performed with mounting the PI312, the following I/O allocation table will be created in the T3.

| <1/0 A1 | location> | | |
|-------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| Unit #0 Slot I/O PU [] 0 [iX+Y 24] 1 [] 2 [] 3 [] 4 [] 5 [] 6 [] 7 [] 8 [] 9 [] | Unit #1 Slot I/O 0 [] 1 [] 2 [] 3 [] 4 [] 5 [] 6 [] 7 [] 8 [] 9 [] 10 [] | Unit #2 Slot I/O 0 [] 1 [] 2 [] 3 [] 4 [] 5 [] 6 [] 7 [] 8 [] 9 [] 10 [] | Unit #3 Slot I/O 0 [] 1 [] 2 [] 3 [] 3 [] 4 [] 5 [] 6 [] 9 [] 10 [] |

(T-PDS screen example - in the case that PI312 is mounted on Slot 0 of Unit 0)

Then, 2 I/O registers, XW(n) and YW(n+1) are assigned to the PI312. In the above example, XW000 and YW001 are assigned.

Note that the I/O type has 'i' designation. It means that the PI312 has interrupt generation function for the T3, also the T3 will not update the assigned I/O registers in the batch I/O processing. To read or write data through the I/O registers, the Direct I/O instruction (FUN235) or the direct I/O designation (I/IW and O/OW instead of X/XW and Y/YW) is necessary.
4. Register Configuration



Register Bit Name Description F - 8 No use (data not defined) _ 1: both phase G and soft-gate for CH 2 are ON 7 CH2 gate status CH2 EXT status 1: EXT input for CH2 is ON 6 5 CH2 less than 1: CH2 count value is less than the set-point-2 set-point-2 1: CH2 count value is greater than the set-point-1 4 CH2 greater than XW(n) set-point- 1 3 CH1 gate status 1: both phase G and soft-gate for CH1 are ON CH1 EXT status 1: EXT input for CH1 is ON 2 CH1 less than 1: CH1 count value is less than the set-point-2 1 set-point-2 CH1 greater than 1: CH1 count value is greater than the set-point-1 0 set-point- 1 F - 7 No use (set to 0) CH2 output-enable Set to 1 to enable CH2's comparison outputs 6 CH2 interrupt-enable Set to 1 to enable CH2's interrupt 5 YW(n+1) 4 CH2 soft-gate Set to 1 to enable CH2's counter function 3 No use (set to 0) Set to 1 to enable CH1's comparison outputs 2 CH1 output-enable 1 CH1 interrupt-enable Set to 1 to enable CH1's interrupt 0 CH1 soft-gate Set to 1 to enable CH1's counter function

The following table shows the functions of I/O registers assigned to the PI312.

4. Register Configuration

4.2 PI312 buffer memory

The PI312's count value, set-point value, operation mode data, and other information are stored in the PI312's buffer memory.

This section explains the buffer memory contents and how to access the buffer memory.

4.2.1 Memory map

The PI312 has the buffer memory that is used to exchange data with T3. The memory map of the buffer memory is as follows.

| Address | Word data |
|---------|-----------|
| | |

| | Channel 1 count value | Channel 1 counter register (24 hit) |
|----------|-----------------------|-------------------------------------------|
| 0 | | Channel i counter register (24-bit) |
| 2 | Channel 1 set-point-1 | Channel 1 upper comparison value (24-bit) |
| 4 | Channel 1 set-point-2 | Channel 1 lower comparison value (24-bit) |
| 6 | Channel 1 hold value | Channel 1 hold register (24-bit) |
| 8 | Channel 2 count value | Channel 2 counter register (24-bit) |
| 10 | Channel 2 set-point-1 | Channel 2 upper comparison value (24-bit) |
| 12 | Channel 2 set-point-2 | Channel 2 lower comparison value (24-bit) |
| 14 | Channel 2 hold value | Channel 2 hold register (24-bit) |
| 16 | Interrupt flag | |
| 17 | Access inhibited | |
| 32 | Channel 1 mode | |
| 33 | Channel 2 mode | |
| 34 63 | Access inhibited | |



The hold value (addresses 7.6 and 15.14) and the interrupt flag (address 16) are reading only. Writing data into these addresses is inhibited. All other addresses are available for both reading and writing. (except the ranges of address 17 through 31 and 34 through 63)

4.2.2 Buffer memory access

T3 can read the PI312's buffer memory contents by using READ instruction (FUN237). Also, T3 can write data into the buffer memory by using WRITE instruction (FUN238).

READ instruction (FUN237)

Expression:

—[(A) READ (B) \rightarrow (C)]—

Operands:

| (A): | I/O register | (XW/YW) | assigned to | the PI312 |
|------|--------------|---------|-------------|-----------|
|------|--------------|---------|-------------|-----------|

(B): Starting address of the buffer memory to be read

(B)+1: Number of words to be read (max. 17 for PI312)

(C): Starting register of the destination

Example:



When R0100 is ON, 16 words of buffer memory data starting with address 0 are read from the PI312 which is allocated to XW000. And the data are stored in D1000 and after.

4. Register Configuration

WRITE instruction (FUN238)

Expression:

—[(A) WRITE (B) \rightarrow (C)]—

Operands:

| (A): | Starting register of the source |
|--------|-----------------------------------------------------|
| (B): | Starting address of the buffer memory to be written |
| (B)+1: | Number of words to be written (max. 6 for PI312) |
| (C): | I/O register (XW/YW) assigned to the PI312 |
| | |

Example:



When R0101 is ON, 2 words of data starting with D2000 (D2000 and D2001) are written into the buffer memory address 32 and 33 of the PI312 which is allocated to YW001.

4.2.3 Count value registers

The addresses 0, 1 and 8, 9 store the count values for channel 1 and channel 2 respectively.

These data can be read into the T3 by READ instruction. Also, the T3 can write (change) the count values by WRITE instruction.

<Channel 1>

| F | | 7 | 0 F | | 0 |
|--------------------------------------------------------------------------|-------------------|---------------------|-----|---------------------|---|
| | No use (always 0) | Count value (upper) | | Count value (lower) | |
| | | | _/\ | | / |
| | Addre | ess 1 | | Address 0 | |
| <c< td=""><td>hannel 2></td><td></td><td></td><td></td><td></td></c<> | hannel 2> | | | | |
| F | | 7 | 0 F | | 0 |
| | No use (always 0) | Count value (upper) | | Count value (lower) | |
| | | | | | / |

Address 9

Address 8

The count value is 24-bit length.

The lower address (address 0 or 8) stores the lower 16-bit of the count value. The higher address (address 1 or 9) stores the upper 8-bit of the count value. These subsequent 2 addresses configure 24-bit count value register. (the count value is 0 to 16777215)

The upper 8 bits of the higher address are all 0. When writing a double-word (32-bit) data into these addresses (presetting the count value), the upper 8 bits should be 0.



In this manual, double-word (32-bit) register is expressed as, upper register · lower register

For example;

D0011.D0010 ... for T3's register

9.8 for PI312's buffer memory address

4. Register Configuration

4.2.4 Upper and lower comparison value registers

The addresses 2 through 5 and 10 through 13 store the comparison values for channel 1 and channel 2 respectively. The upper comparison value is called set-point-1, and the lower comparison value is called set-point-2. The function of these data is dependent on the counter operation mode.

These data can be written from the T3 by WRITE instruction. Also, the T3 can read these data by READ instruction.

| F | 8 7 | 0 F | | 0 |
|----------------------------------------------------------------------------------------------|--------------------|-----|---------------------|---|
| No use (always 0) | Set-point-1 (upper | r) | Set-point-1 (lower) | |
| \backslash | | | | / |
| Ad | dress 3 | | Address 2 | |
| <channel -="" 1="" set-po<="" td=""><td>bint-2></td><td></td><td></td><td></td></channel> | bint-2> | | | |
| F | 8 7 | 0 F | | 0 |
| No use (always 0) | Set-point-2 (upper | r) | Set-point-2 (lower) | |
| \ | | _/\ | | / |
| Ad | dress 5 | | Address 4 | |
| <channel -="" 2="" set-po<="" td=""><td>pint-1></td><td></td><td></td><td></td></channel> | pint-1> | | | |
| F | 8 7 | 0 F | | 0 |
| No use (always 0) | Set-point-1 (upper | r) | Set-point-1 (lower) | |
| \ | | _/\ | | / |
| Ado | dress 11 | | Address 10 | |
| <channel -="" 2="" set-pc<="" td=""><td>bint-2></td><td></td><td></td><td></td></channel> | bint-2> | | | |
| F | 8 7 | 0 F | | 0 |
| No use (always 0) | Set-point-2 (upper | r) | Set-point-2 (lower) | |
| \ | | _/\ | | / |
| Ado | dress 13 | | Address 12 | |

<Channel 1 - set-point-1>

The comparison value (set-point-1 or -2) is 24-bit length. The lower address stores the lower 16-bit of the comparison value. The higher address stores the upper 8-bit of the comparison value. These subsequent 2 addresses configure 24-bit comparison value register. The upper 8 bits of the higher address are all 0. When writing a double-word (32-bit) data into these addresses (setting the comparison value), the upper 8 bits should be 0.

4.2.5 Hold value registers

The addresses 6, 7 and 14,15 store the hold values for channel 1 and channel 2 respectively.

These data can be read into the T3. Writing data into these addresses is prohibited.

<Channel 1>

| F | | 7 | 0 F | | 0 |
|--------------------------------------------------------------------------|-------------------|--------------------|------|--------------------|---|
| | No use (always 0) | Hold value (upper) | | Hold value (lower) | |
| | | | _/ \ | | / |
| | Addre | ess 7 | | Address 6 | |
| <c< td=""><td>hannel 2></td><td></td><td></td><td></td><td></td></c<> | hannel 2> | | | | |
| F | | 7 | 0 F | | 0 |
| | No use (always 0) | Hold value (upper) | | Hold value (lower) | |
| | | | _/ \ | | / |
| | Addre | ess 15 | | Address 14 | |

The hold value is 24-bit length.

The lower address stores the lower 16-bit of the hold value.

The higher address stores the upper 8-bit of the hold value.

These subsequent 2 addresses configure 24-bit hold value register.

The upper 8 bits of the higher address are all 0.

4. Register Configuration

4.2.6 Interrupt flags

The bit 0 and the bit 1 of the address 16 function as the interrupt flags for channel 1 and channel 2 respectively.

When an interrupt is generated by the PI312, the corresponding interrupt program in the T3 is activated immediately. In the interrupt program, read the interrupt flags to check which channel generates the interrupt.

Also, by reading the interrupt flags, the PI312 recognizes the interrupt has been accepted by the T3. Until the interrupt flags are read, the PI312 carnot generate the next interrupt.

These flags can be read by READ instruction. Writing data into this addresses is prohibited.



The interrupt flags are reset to 0 by reading this address.

4.2.7 Operation mode registers

The channel 1 operation mode can be set by writing an appropriate data into the address 32. And the channel 2 operation mode can be set by writing an appropriate data into the address 33.

Operation mode setting is important to use the PI312. See section 5 for how to set the operation mode.

The operation mode registers can also be read by READ instruction. It is recommended to read and check the data after setting the operation mode.



Section 5

Operation Mode Setting

- 5.1 Mode setting overview
- 5.2 Jumper plug setting
- 5.3 Operation mode register setting

5.1 Mode setting overview

The PI312 has total 9 operation modes.

- (1) Quadrature bi-pulse counter mode
- (2) Up/down pulse counter mode
- (3) Auto-reset universal counter mode
- (4) Universal counter mode
- (5) Speed counter mode
- (6) Programmable interval timer mode
- (7) Gate-ON timer mode
- (8) Slave counter mode
- (9) Slave timer mode

As for above (1) through (7) modes, the operation mode can be set individually for channel 1 and channel 2. For example, you can set channel 1 to the quadrature bi-pulse counter and channel 2 to the speed counter.

On the other hand, when above (8) or (9) mode is used, channel 1 and channel 2 work relatively. In this case, channel 1 must be set to (3) auto-reset universal counter mode. For example, when you use the slave counter mode, you should set channel 1 to the auto-reset universal counter and channel 2 to the slave counter.

To set the operation mode, jumper plugs and the operation mode register in the Pl312's buffer memory are used.

The jumper plugs are used to select either individual operation (above (1) through (7) modes) or relative operation (above (8) and (9) modes).

There are 2 operation mode registers in the buffer memory. One is for channel 1 and the other is for channel 2. By writing a mode data into this register, the operation mode setting for each channel is established.

5.2 Jumper plug setting

2 jumper plugs are provided on the PI312's printed circuit board. Use tweezers to change the settings.



J2 is used to select either individual operation (other than slave counter/timer mode) or relative operation (slave counter/timer mode).

| J2 | Short | Individual operation |
|----|-------------------|--------------------------------------------------|
| | (factory setting) | (for modes (1) through (7) on the previous page) |
| | Open | Relative operation |
| | | (for modes (8) and (9) on the previous page) |

J1 is used to select the PI312's initialization mode.

| J1 | A side (factory setting) | PI312 is initialized at both power on and the beginning of T3 RUN. |
|----|-----------------------------|--------------------------------------------------------------------|
| | B side | PI312 is initialized only at power on. |

By the initialization, the operation mode is reset to the up/down pulse counter mode, and the contents of the PI312's buffer memory is cleared to 0.

5.3 Operation mode register setting

To use the PI312, it is important to set (write) a correct data into the operation mode register which is allocated on the PI312's buffer memory. (Refer to section 4.2.7)

Operation mode register:

<Channel 1>

| | F | Е | D | С | В | А | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|---|----|-----|-------|-----|--------|-----|---|---|---|-------|-------|------|--------|---|---|
| 32 | | No | use | (data | not | define | ed) | | | (| Opera | ation | mode | e data | a | |

<Channel 2>

| | F | Е | D | С | В | А | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|---|----|-----|-------|-----|-------|-----|---|---|---|-------|-------|------|--------|---|---|
| 33 | | No | use | (data | not | defin | ed) | | | (| Opera | ation | mode | e data | a | |

The table on the next page shows the operation mode data to be written into the operation mode register for setting each mode.

To write the data into the operation mode register, WRITE instruction (FUN238) is used.

| Operatio | on mode | Pulse count | Internal clock | Operation mod | | |
|------------------|---------------|-------------|----------------|---------------|-------|--|
| | | mode | mode selection | | ata | |
| Quadrature bi-p | ulse counter | Normal | No use | H0002 | (2) | |
| mode | | Precision | No use | H0042 | (66) | |
| Up/down pulse | counter mode | Normal | No use | H0000 | (0) | |
| | | Precision | No use | H0040 | (64) | |
| Auto-reset unive | ersal counter | Normal | No use | H0081 | (129) | |
| mode | | Precision | No use | H00C1 | (193) | |
| Universal count | er mode | Normal | No use | H0001 | (1) | |
| | | Precision | No use | H0041 | (65) | |
| Speed counter | 0.01 second | Normal | No use | H0005 | (5) | |
| mode | sampling | Precision | No use | H0045 | (69) | |
| | 0.1 second | Normal | No use | H000D | (13) | |
| | sampling | Precision | No use | H004D | (77) | |
| Programmable i | nterval timer | Normal | 1 kHz | H0091 | (145) | |
| mode | | | 10 kHz | H00A1 | (161) | |
| | | | 100 kHz | H00B1 | (177) | |
| | | Precision | 1 kHz | H00D1 | (209) | |
| | | | 10 kHz | H00E1 | (225) | |
| | | | 100 kHz | H00F1 | (241) | |
| Gate-ON timer r | node | Normal | 1 kHz | H0011 | (17) | |
| | | | 10 kHz | H0021 | (33) | |
| | | | 100 kHz | H0031 | (49) | |
| | | Precision | 1 kHz | H0051 | (81) | |
| | | | 10 kHz | H0061 | (97) | |
| | | | 100 kHz | H0071 | (113) | |
| Slave counter m | node | Normal | No use | H0001 | (1) | |
| | | Precision | No use | H0041 | (65) | |
| Slave timer mod | le | Normal | 1 kHz | H0011 | (17) | |
| | | | 10 kHz | H0021 | (33) | |
| | | | 100 kHz | H0031 | (49) | |
| | | Precision | 1 kHz | H0051 | (81) | |
| | | | 10 kHz | H0061 | (97) | |
| | | | 100 kHz | H0071 | (113) | |



(1) For the pulse count mode, refer to section 1.2.2.
(2) The number in brackets () on the operation mode data column shows the decimal value of the operation mode data.

T3 sample programs to set the operation modes are shown below. In these sample programs, the PI312's operation modes are set at the first scan of the T3 program execution.

Sample 1:

This program sets channel 1 to the quadrature bi-pulse counter of precision pulse count mode, and channel 2 to the 0.01 second speed counter of normal pulse count mode.

In this case, the jumper plug J2 should be shorted.

It is assumed that the PI312 is allocated to XW000 and YW001.

| 1 | |
|---|----------------------------------------|
| | [88832 HOV D4588]-[88882 HOV D4581]- |
| | [D0010 WRITE D4500 → XW000] |

By executing this program, the data 66 (H0042) and 5 (H0005) are written into the addresses 32 and 33 of the PI312's buffer memory respectively.

Sample 2:

This program sets channel 1 to the auto-reset universal counter of normal pulse count mode, and channel 2 to the slave timer with using 10 kHz clock of precision pulse count mode.

In this case, the jumper plug J2 is opened.

It is assumed that the PI312 is allocated to XW000 and YW001.

| 1 | 11 | -{ 00129 | 9 MOV | D0010]-[| 00097 | MOV | 00011] |
|---|----|----------|-------|------------------|-------|-------|--------|
| | - | -E 00034 | 2 MOV | D4500]{[| 00002 | MOV | D4501] |
| | - | | WRIT | £ 04500 | → X | N888) |] |

By executing this program, the data 129 (H0081) and 97 (H0061) are written into the addresses 32 and 33 of the PI312's buffer memory respectively.

Section 6

Function Details

- 6.1 Quadrature bi-pulse counter mode
- 6.2 Up/down pulse counter mode
- 6.3 Auto-reset universal counter mode
- 6.4 Universal counter mode
- 6.5 Speed counter mode
- 6.6 Programmable interval timer mode
- 6.7 Gate-ON timer mode
- 6.8 Slave counter mode
- 6.9 Slave timer mode

6.1 Quadrature bi-pulse counter mode

(1) Mode setting

Jumper plug (J2) = Short

Operation mode data = H0002 (2) ... Normal count mode = H0042 (66) ... Precision count mode

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function |
|---------|---------------------------------------------------------|
| Phase A | Quadrature pulses Counting up when phase A precedes |
| Phase B | Counting down when phase B precedes |
| Phase G | Used to enable the counter operation |
| | (enabled while both phase G and soft-gate are ON) |
| Phase M | Used to clear the count value |
| EXT | (cleared at the rising edge of phase M while EXT is ON) |
| S1 | Hardware comparison output |
| | Comes ON when count value > set-point-1 |
| S2 | Hardware comparison output |
| | Comes ON when count value < set-point-2 |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|-----------------------------------------------------|
| | (CH1/CH2) | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) |
| Set-point-1 | 3.2 / 11.10 | Used to set the upper comparison value (read/write) |
| Set-point-2 | 5·4 / 13·12 | Used to set the lower comparison value (read/write) |
| Hold value | 7.6 / 15.14 | Stores the count value at the gate comes OFF (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function |
|------------------|---------------------------|---------------------------------------------------|
| Soft-gate | 0 / 4 | Used to enable the counter operation |
| | | (enabled while both phase G and soft-gate are ON) |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function |
| Output-enable | 2/6 | Set to ON to enable hardware comparison outputs |

(5) Operation

PI312 counts the pulses whose phases are shifted 90° each other. When phase A pulse precedes against phase B pulse, the PI312 counts up (increase). On the other hand, when phase B pulse precedes, the PI312 counts down (decrease).

PI312 can count up to 50 kHz pulses. Therefore the maximum counting speed is as follows.

Normal count mode: 50 k counts per second Precision count mode: 200 k counts per second

This mode function is enabled while both phase G and soft-gate are ON. (even when the either is OFF, counting is not stopped)

The count value can be changed by directly writing a data into the buffer memory. Also,

the count value is cleared to 0 by hardware at the following timing.

- a) At the moment of both phase G and soft-gate come ON
- b) At the moment of phase M comes ON while EXT is ON (100 ms or more of EXT ON state is necessary before phase M comes ON)

When the count value is increased by 1 in the upper limit value (16777215), it is reset to 0. When the count value is decreased by 1 in the lower limit value (0), it is reset to the upper limit value (16777215).

When the output-enable bit in the command register (YW) is ON, the hardware comparison outputs (S1 and S2) are enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON. And when the count value is smaller than the set-point-2, S2 comes ON.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1 in counting up or it reaches the set-point-2 in counting down, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately. For details of the interrupt function, refer to section 7.

When phase G or soft-gate comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the quadrature bi-pulse counter mode (precision) for channel 1

| 1 | THE BOOGG HOV DOB10] |
|---|-----------------------------------------|
| | -[88832 MOV RU858]-[88881 MOV RU851]- |
| | |

At the beginning of RUN mode (at the first scan), the mode data 66 (H0042) is written into the address 32 (CH1 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = OFF Output-enable (Y0012) = ON



When R0100 is ON, Y0010 and Y0012 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

Channel 1 Set-point-1 = 150000 Set-point-2 = 200

| 1 | R0101 ⊢ † | -[0000150000 DMOV D0013.D0012] |
|---|-----------------|----------------------------------------|
| | | -[8898888288 DMOV D8815.D8814] |
| | | -[00002 MOV RN050]-[00004 MOV RN051] |
| | _ L | -[D0012 WRITE RW050 → XW000] |

At the rising edge of R0101 coming ON, the data 150000 and 200 are written into the addresses 3.2 (CH1 set-point-1) and 5.4 (CH1 set-point-2).

• Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101.D0100.

To use the status register (XW000), direct I/O instruction is necessary in the program.

6.2 Up/down pulse counter mode

(1) Mode setting

Jumper plug (J2) = Short

Operation mode data = H0000 (0) ... Normal count mode = H0040 (64) ... Precision count mode

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function |
|---------|---------------------------------------------------------|
| Phase A | Counting up pulse |
| Phase B | Counting down pulse |
| Phase G | Used to enable the counter operation |
| | (enabled while both phase G and soft-gate are ON) |
| Phase M | Used to clear the count value |
| EXT | (cleared at the rising edge of phase M while EXT is ON) |
| S1 | Hardware comparison output |
| | Comes ON when count value > set-point-1 |
| S2 | Hardware comparison output |
| | Comes ON when count value < set-point-2 |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|-----------------------------------------------------|
| | (CH1/CH2) | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) |
| Set-point-1 | 3.2 / 11.10 | Used to set the upper comparison value (read/write) |
| Set-point-2 | 5·4 / 13·12 | Used to set the lower comparison value (read/write) |
| Hold value | 7.6 / 15.14 | Stores the count value at the gate comes OFF (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function |
|------------------|---------------------------|---------------------------------------------------|
| Soft-gate | 0 / 4 | Used to enable the counter operation |
| | | (enabled while both phase G and soft-gate are ON) |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function |
| Output-enable | 2/6 | Set to ON to enable hardware comparison outputs |

(5) Operation

PI312 counts the pulses phase A and phase B. Phase A is counting up (increase), and phase B is counting down (decrease). When both phase A and phase B come ON simultaneously, counting is not executed.

In the normal count mode, PI312 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.

This mode function is enabled while both phase G and soft-gate are ON. (even when the either is OFF, counting is not stopped)

The count value can be changed by directly writing a data into the buffer memory. Also,

the count value is cleared to 0 by hardware at the following timing.

- a) At the moment of both phase G and soft-gate come ON
- b) At the moment of phase M comes ON while EXT is ON (100 ms or more of EXT ON state is necessary before phase M comes ON)

When the count value is increased by 1 in the upper limit value (16777215), it is reset to 0. When the count value is decreased by 1 in the lower limit value (0), it is reset to the upper limit value (16777215).

When the output-enable bit in the command register (YW) is ON, the hardware comparison outputs (S1 and S2) are enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON. And when the count value is smaller than the set-point-2, S2 comes ON.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1 in counting up or it reaches the set-point-2 in counting down, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately. For details of the interrupt function, refer to section 7.

When phase G or soft-gate comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the up/down pulse counter mode (normal) for channel 1

| 1 | [88888 NOV DEB18] | |
|---|-----------------------------------------|--|
| | -[88832 HOV RU858]-[88881 MOV RU851]- | |
| | | |

At the beginning of RUN mode (at the first scan), the mode data 0 is written into the address 32 (CH1 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = OFF Output-enable (Y0012) = ON



When R0100 is ON, Y0010 and Y0012 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

Channel 1 Set-point-1 = 150000 Set-point-2 = 200

| 1 | R0101 → † | [0000150000 DMOV D0013.D0012] |
|---|----------------|----------------------------------------|
| | - | -[000000200 DMOV D0015.D0014] |
| | - | -[00002 MOV RW050] [00004 MOV RW051] |
| | - | _[D0012 WRITE RW050 → XW000] |

At the rising edge of R0101 coming ON, the data 150000 and 200 are written into the addresses 3.2 (CH1 set-point-1) and 5.4 (CH1 set-point-2).

• Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101.D0100.

To use the status register (XW000), direct I/O instruction is necessary in the program.

6.3 Auto-reset universal counter mode

(1) Mode setting

Jumper plug (J2) = Short

Operation mode data = H0081 (129) ... Normal count mode = H00C1 (193) ... Precision count mode

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function | |
|---------|----------------------------------------------------------------------------------------|--|
| Phase A | Counting up pulse | |
| Phase B | No use | |
| Phase G | Used to enable the counter operation (enabled while both phase G and soft-gate are ON) | |
| Phase M | No use | |
| EXT | No use | |
| S1 | No use | |
| S2 | No use | |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|-----------------------------------------------------|
| Countivalue | | Stores the count value (read/write) |
| | 1.0/9.0 | |
| Set-point-1 | 3.2 / 11.10 | Used to set the reset point (read/write) |
| Set-point-2 | 5.4 / 13.12 | No use |
| Hold value | 7.6 / 15.14 | Stores the count value at the gate comes OFF (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function |
|------------------|---------------------------|---------------------------------------------------|
| Soft-gate | 0 / 4 | Used to enable the counter operation |
| - | | (enabled while both phase G and soft-gate are ON) |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function |
| Output-enable | 2/6 | No use |

(5) Operation

PI312 counts up by the single phase pulses into phase A.

In the normal count mode, PI312 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.

This mode function is enabled while both phase G and soft-gate are ON. (even when the either is OFF, counting is not stopped)

The count value can be changed by directly writing a data into the buffer memory.

When the count value reaches the set-point-1, the count value is reset to 0 (zero). The set-point-1 can be set in the range of 1 to 16777215.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately. For details of the interrupt function, refer to section 7.

When phase G or soft-gate comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

Setting the auto-reset universal counter mode (normal) for channel 1

| 1 | | 919] |
|---|-------------------|------------------------|
| | | 858]{ 88881 MOV RW851] |
| | . LOGO10 WRITE RW | W850 → XW880] |

At the beginning of RUN mode (at the first scan), the mode data 129 (H0081) is written into the address 32 (CH1 mode) of the buffer memory.

Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = ON Output-enable (Y0012) = OFF

| | R0100 | | Y9010 |
|---|-----------|-------------|-------|
| | | | ¥9011 |
| 2 | - 1/0 | (82) XU888] | |
| - | L | | |

When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

Writing the set-point data

Channel 1

Set-point-1 = 90000R0101 |||__[0000090000 DMOV D0013.D0012]--- \dashv -[00002 MOV RW050][00002 MOV RW051]-└_[D0012 WRITE RW050 → XW000]--

At the rising edge of R0101 coming ON, the data 90000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the count value

When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101.D0100.

To use the status register (XW000), direct I/O instruction is necessary in the program.

6.4 Universal counter mode

(1) Mode setting

Jumper plug (J2) = Short Operation mode data = H0001 (1) ... Normal count mode = H0041 (65) ... Precision count mode

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function | |
|---------|---------------------------------------------------|--|
| Phase A | Counting up pulse | |
| Phase B | No use | |
| Phase G | Used to enable the counter operation | |
| | (enabled while both phase G and soft-gate are ON) | |
| Phase M | No use | |
| EXT | No use | |
| S1 | Hardware comparison output | |
| | Comes ON when count value > set-point-1 | |
| S2 | No use | |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|-----------------------------------------------------|
| | (CH1/CH2) | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) |
| Set-point-1 | 3·2 / 11·10 | Used to set the comparison value (read/write) |
| Set-point-2 | 5·4 / 13·12 | No use |
| Hold value | 7·6 / 15·14 | Stores the count value at the gate comes OFF (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function |
|------------------|---------------------------|---------------------------------------------------|
| Soft-gate | 0 / 4 | Used to enable the counter operation |
| | | (enabled while both phase 6 and solt-gate are ON) |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function |
| Output-enable | 2/6 | Set to ON to enable hardware comparison output |

(5) Operation

PI312 counts up by the single phase pulses into phase A.

In the normal count mode, PI312 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.

This mode function is enabled while both phase G and soft-gate are ON. (even when the either is OFF, counting is not stopped)

The count value can be changed by directly writing a data into the buffer memory.

When the count value exceeds the upper limit value (16777215), it is reset to 0 (zero).

When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately. It is also possible to change the set-point-1 during operation. For details of the interrupt function, refer to section 7.

When phase G or soft-gate comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

Setting the universal counter mode (normal) for channel 1

| 1 | |
|---|----------------------------------------|
| | - F 88832 NOV BURSET 88881 NOV BURS17- |
| | |
| | |

At the beginning of RUN mode (at the first scan), the mode data 1 is written into the address 32 (CH1 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

Channel 1

Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = ON Output-enable (Y0012) = OFF



When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

Writing the set-point data

Channel 1

Set-point-1 = 90000R0101 -[0000090000 DMOV D0013.D0012]---1 - F 내다 [00002 MOV RW050][00002 MOV RW051]--[D0012 WRITE RW050 → XW000]-

At the rising edge of R0101 coming ON, the data 90000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the count value

When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101.D0100.

To use the status register (XW000), direct I/O instruction is necessary in the program.

6.5 Speed counter mode

(1) Mode setting

```
 \begin{array}{l} \text{Jumper plug (J2) = Short} \\ \text{Operation mode data = H0005 (5) } \dots & 0.01 \text{ s sampling} \\ & = H000D (13) \dots & 0.1 \text{ s sampling} \\ & = H0045 (69) \dots & 0.01 \text{ s sampling} \\ & = H004D (77) \dots & 0.1 \text{ s sampling} \end{array} \right) \text{Precision count mode}
```

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function |
|---------|-----------------------------------------|
| Phase A | Counting up pulse |
| Phase B | No use |
| Phase G | No use |
| Phase M | No use |
| EXT | No use |
| S1 | Hardware comparison output |
| | Comes ON when count value > set-point-1 |
| S2 | No use |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|--------------------------------------------------|
| | (CH1/CH2) | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) |
| Set-point-1 | 3.2 / 11.10 | Used to set the comparison value (read/write) |
| Set-point-2 | 5·4 / 13·12 | No use |
| Hold value | 7.6 / 15.14 | Stores the count value in a sampling time (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function |
|------------------|---------------------------|---------------------------------------------------------|
| Soft-gate | 0 / 4 | Used to enable the counter operation (enabled while ON) |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function |
| Output-enable | 2/6 | Set to ON to enable hardware comparison output |

(5) Operation

PI312 counts the single phase pulses into phase A during the specified sampling time. The sampling time can be selected from 0.01 second or 0.1 second.

In the normal count mode, PI312 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.

This mode function is enabled while soft-gate is ON. (even when it is OFF, counting is not stopped)

The count value in a sampling time is transferred into the hold register. By reading the hold register, the pulse rate can be measured.

When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 will be started immediately. For details of the interrupt function, refer to section 7.



 ΔT : sampling time = 0.01s or 0.1s

(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the 0.1 second sampling speed counter mode (normal) for channel 1



At the beginning of RUN mode (at the first scan), the mode data 13 (H000D) is written into the address 32 (CH1 mode) of the buffer memory.
• Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = ON Output-enable (Y0012) = OFF



When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

| Channel 1 | Set-point-1 = 3000 |
|-----------|-----------------------------------------------------------------------------|
| 1 | -[0000003000 DMOV D0013.D00012] -[000082 MOV RW050]{ 000082 MOV RW051] |
| | -[D0012 WRITE RW050 → XW000] |

At the rising edge of R0101 coming ON, the data 3000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the hold value



When R0100 is ON, the hold value is read and stored in the double-word register D0103.D0102.

6.6 Programmable interval timer mode

(1) Mode setting

```
Jumper plug (J2) = Short
```

```
Operation mode data = H0091 (145) ... 1 kHz clock
= H00A1 (161) ... 10 kHz clock
= H00B1 (177) ... 100 kHz clock
= H00D1 (209) ... 1 kHz clock
= H00E1 (225) ... 10 kHz clock
= H00F1 (241) ... 100 kHz clock
```

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function |
|---------|-----------------------------------------------------------------------------------|
| Phase A | No use |
| Phase B | No use |
| Phase G | Used to enable the operation (enabled while both phase G and soft-gate are ON) |
| Phase M | No use |
| EXT | No use |
| S1 | No use |
| S2 | No use |

(3) Buffer memory

| Name | Address | Function | |
|----------------|-------------|-----------------------------------------------------|--|
| | (CH1/CH2) | | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) | |
| Set-point-1 | 3·2 / 11·10 | Used to set the interval (read/write) | |
| Set-point-2 | 5·4 / 13·12 | No use | |
| Hold value | 7·6 / 15·14 | Stores the count value at the gate comes OFF (read) | |
| Interrupt flag | 16 | Used for interrupt function (read) | |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) | |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function | |
|------------------|---------------------------|---------------------------------------------------|--|
| Soft-gate | 0 / 4 | Used to enable the operation | |
| | | (enabled while both phase G and soft-gate are ON) | |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function | |
| Output-enable | 2/6 | No use | |

(5) Operation

PI312 generates an interrupt every specified interval time. The interval time is measured by counting PI312's internal clock pulses. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

In the normal count mode, PI312 counts at the rising edge of the internal clock pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the internal clock pulse. The table below shows the time units which increases the count value by 1.

| Count mode | Internal clock | Time units (= 1 count) | |
|---------------|----------------|------------------------|--|
| Normal | 1 kHz | 1 ms | |
| | 10 kHz | 0.1 ms | |
| | 100 kHz | 0.01 ms | |
| Precision | 1 kHz | 0.5 ms | |
| | 10 kHz | 0.05 ms | |
| | 100 kHz | 0.005 ms | |

This mode function is enabled while both phase G and soft-gate are ON. (even when the either is OFF, counting is not stopped)

When the count value reaches the set-point-1, the count value is reset to 0 (zero). The set-point-1 can be set in the range of 1 to 16777215.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1, the PI312 generates interrupt signal for the T3. Therefore PI312 functions as cyclic interrupt generator.

For example, when the set-point-1 is 285 in 10 kHz normal count mode, the PI312 generates interrupt every 28.5 ms.

When phase G or soft-gate comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the programmable interval timer with 10 kHz clock (normal) for channel 1



At the beginning of RUN mode (at the first scan), the mode data 161 (H00A1) is written into the address 32 (CH1 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = ON Output-enable (Y0012) = OFF



When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

Channel 1 Set-point-1 = 28300

At the beginning of RUN mode (at the first scan), the data 28300 is written into the addresses 3.2 (CH1 set-point-1). Resulting the PI312 generates interrupt every 2.83 seconds.

When an interrupt is generated, corresponding I/O interrupt program in the T3 will be started immediately. For details of the interrupt function, refer to section 7.

6.7 Gate-ON timer mode

(1) Mode setting

```
Jumper plug (J2) = Short

Operation mode data = H0011 (17) ... 1 kHz clock

= H0021 (33) ... 10 kHz clock

= H0031 (49) ... 100 kHz clock

= H0051 (81) ... 1 kHz clock

= H0061 (97) ... 10 kHz clock

= H0071 (113) ... 100 kHz clock
```

This mode can be set individually for channel 1 and channel 2.

(2) External signals

| Signal | Function |
|---------|-------------------------------------------|
| Phase A | No use |
| Phase B | No use |
| Phase G | Gate signal whose ON duration is measured |
| Phase M | No use |
| EXT | No use |
| S1 | Hardware comparison output |
| | Comes ON when count value > set-point-1 |
| S2 | No use |

(3) Buffer memory

| Name | Address | Function |
|----------------|-------------|-----------------------------------------------------|
| | (CH1/CH2) | |
| Count value | 1.0 / 9.8 | Stores the count value (read/write) |
| Set-point-1 | 3.2 / 11.10 | Used to set the comparison value (read/write) |
| Set-point-2 | 5.4 / 13.12 | No use |
| Hold value | 7·6 / 15·14 | Stores the count value in a gate ON duration (read) |
| Interrupt flag | 16 | Used for interrupt function (read) |
| Mode register | 32 / 33 | Used to set the operation mode (read/write) |

(4) Command register (YW)

| Name | Bit position (CH1/CH2) | Function | |
|------------------|---------------------------|------------------------------------------------|--|
| Soft-gate | 0 / 4 | Used to enable the operation | |
| | | (enabled while soft-gate is ON) | |
| Interrupt-enable | 1 / 5 | Set to ON to enable interrupt function | |
| Output-enable | 2/6 | Set to ON to enable hardware comparison output | |

(5) Operation

PI312 measures the time duration of phase G ON state. The time is measured by counting PI312's internal clock pulses. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

In the normal count mode, PI312 counts at the rising edge of the internal clock pulse. On the other hand, in the precision count mode, PI312 counts at both rising and falling edges of the internal clock pulse. The table below shows the time units which increases the count value by 1.

The count rage is 1 to 16777215. The countable duration is also shown in the table.

| Count mode | Internal clock | Time units (= 1 count) | Countable duration |
|---------------|----------------|------------------------|-------------------------|
| Normal 1 kHz | | 1 ms | 1 ms to 16777.215 s |
| | 10 kHz | 0.1 ms | 0.1 ms to 1677.7215 s |
| | 100 kHz | 0.01 ms | 0.01 ms to 167.77215 s |
| Precision | 1 kHz | 0.5 ms | 0.5 ms to 8388.6075 s |
| | 10 kHz | 0.05 ms | 0.05 ms to 838.86075 s |
| | 100 kHz | 0.005 ms | 0.005 ms to 83.886075 s |

This mode function is enabled while soft-gate is ON.

When the phase G signal is changed to ON, the counting is started from 0. Then the phase G signal is changed to OFF, the count value is transferred to the hold register. For example, if the hold register value is 7863 under the setting of 10 kHz precision mode, it means that the phase G ON duration was;

7863 × 0.05 ms = 393.15 ms

When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.

When the interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the count value reaches the set-point-1, the PI312 generates an interrupt signal for the T3.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the gate-ON timer mode (10 kHz, precision) for channel 1

| 1 | The comparison of the comparis | |
|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| | - [88832 MOV RW858] [88881 MOV RW851] | |
| | [D0010 WRITE RW050 → XW000] | |

At the beginning of RUN mode (at the first scan), the mode data 97 (H0061) is written into the address 32 (CH1 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

Channel 1 Soft-gate (Y0010) = ON Interrupt-enable (Y0011) = ON Output-enable (Y0012) = OFF



When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

| Channel 1 | Set-point-1 = 3000 |
|-----------|-------------------------------------------------------------------------|
| 1 | [0000003000 DMOV D0013.D0012] -[00002 MOV RW050]{ 00002 MOV RW051] |
| - | [D0012 WRITE RW050 → XW000] |

At the rising edge of R0101 coming ON, the data 3000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the hold value



When X0003 (CH1 gate status) is changed to OFF, the hold value is read and stored in the double-word register D0103 D0102.

To use the status register (XW000), direct I/O instruction is necessary in the program.

6.8 Slave counter mode

(1) Mode setting

Jumper plug (J2) = Open

Operation mode data

| Channel 1 | | | Channel 2 | | |
|--------------------------------|-------------|--|-----------------|----------------|--|
| (Auto-reset universal counter) | | | (Slave counter) | | |
| H0081 (129) | Normal mode | | H0001 (1) | Normal mode | |
| H00C1 (193) Precision mode | | | H0041 (65) | Precision mode | |

In this mode, channel 2 works relatively with channel 1.

(2) External signals

| Signal | Channel 1 | Channel 2 |
|---------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| Phase A | Counting up pulse | Counting up pulse |
| Phase B | No use | No use |
| Phase G | Used to enable the operation (enabled while both phase G and soft-gate are ON) | No use |
| Phase M | No use | No use |
| EXT | No use | No use |
| S1 | No use | Hardware comparison output ON when count value > set-point- 1 |
| S2 | No use | No use |

(3) Buffer memory

| Name | Channel 1 | | Channel 2 | | |
|----------------|-----------|-----------------------|-----------|-----------------------|--|
| | Address | Function | Address | Function | |
| Count value | 1.0 | Stores the count | 9.8 | Stores the count | |
| | | value (read/write) | | value (read/write) | |
| Set-point-1 | 3.2 | Used to set the reset | 11.10 | Used to set the | |
| | | point (read/write) | | comparison value | |
| | | | | (read/write) | |
| Set-point-2 | 5.4 | No use | 13.12 | No use | |
| Hold value | 7.6 | Stores the count | 15.14 | Stores the count | |
| | | value at the gate | | value in the CH1 | |
| | | comes OFF (read) | | reset interval (read) | |
| Interrupt flag | 16 | Used for interrupt | 16 | Used for interrupt | |
| | | function (read) | | function (read) | |
| Mode register | 32 | Used to set the | 33 | Used to set the | |
| | | operation mode | | operation mode | |
| | | (read/write) | | (read/write) | |

| Name | Channel 1 | | Channel 2 | | |
|----------------------|-----------|--------------------------------------------------------------------------------------------|-----------|------------------------------------------------------|--|
| | Bit | Function | Bit | Function | |
| Soft-gate | 0 | Used to enable the operation (enabled while both phase G and soft-gate are ON) | 4 | No use | |
| Interrupt- enable | 1 | Set to ON to enable interrupt function for CH1 | 5 | Set to ON to enable interrupt function for CH2 | |
| Output-enable | 2 | No use | 6 | Set to ON to enable hardware comparison output | |

(4) Command register (YW)

(5) Operation

In this mode, the channel 2 works relatively with the channel 1 operation. The channel 1 is set as the auto-reset universal counter mode. The channel 2 counts the single phase pulses into phase A in the channel 1 reset interval.

When the channel 1 count value reaches the channel 1's set-point-1, the channel 2 count value is transferred into the channel 2's hold register, and both channel 1 and channel 2 count values are reset to 0.

Therefore, this mode can be used to measure the frequency ratio of channel 1 and channel 2 pulses.

This mode function is enabled while both phase G and soft-gate for channel 1 are ON. (even when the either is OFF, counting is not stopped)

When the channel 2's output-enable bit in the command register (YW) is ON, the hardware comparison output (2S1) is enabled. In this condition, when the channel 2 count value is greater than the channel 2 set-point-1, 2S1 comes ON.

When the channel 2's interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the channel 2 count value reaches the channel 2 set-point-1, the PI312 generates an interrupt signal for the T3.

For details of the channel 1 counter operation, refer to section 6.3 Auto-reset universal counter mode.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the auto-reset universal counter (normal) for channel 1, and the slave counter (normal) for channel 2

| 1 | 1 [88129 MOV D6818][88881 MOV D6811] |
|---|-----------------------------------------|
| | - [88832 MOV RW858] [88882 MOV RW851] |
| | |

At the beginning of RUN mode (at the first scan), the mode data 129 (H0081) is written into the address 32 (CH1 mode) and the mode data 1 (H0001) is written into the address 33 (CH2 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

| Channel 1: | Soft-gate (Y0010) = ON |
|------------|--------------------------------|
| | Interrupt-enable (Y0011) = ON |
| | Output-enable (Y0012) = OFF |
| Channel 2: | Soft-gate (Y0014) = OFF |
| | Interrupt-enable (Y0015) = OFF |
| | Output-enable (Y0016) = OFF |
| | |

| | R0100 | | Y0010 |
|---|-------|-------------|-------|
| 1 | Π | | Y9011 |
| t | | | () |
| z | { 1/0 | (02) XW000] | |

When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

| Channel 1 | Set-point-1 = 3000 |
|--------------|----------------------------------------|
| 1 101 1 | [0000003000 DMOV D0013.D0012] |
| - | -[00002 HOU RW050]-[00002 MOU RW051] |

At the rising edge of R0101 coming ON, the data 3000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the channel 2 hold value in the interrupt program

| 1-[| 88816 MOV RW868]{ 88881 MOV RW861] |
|------------|-----------------------------------------|
| 2-[X R0 | (W888 READ RW868 → RW888] 9888 |
| 3 | - [88814 MOV RW868] [88882 MOV RW861] |
| 4 | -[IRET]- |

When the channel 1 generates an interrupt, the above interrupt program is executed. In this interrupt program, the interrupt flag (address 16) is read at first. Then the channel 2 hold value (address 15·14) is read and stored in the double-word register D0103·D0102.

Refer to section 7 for more information about the interrupt function.

6.9 Slave timer mode

(1) Mode setting

Jumper plug (J2) = Open

Operation mode data

| Channel 1 | | | |
|--------------------------------|--|--|--|
| (Auto-reset universal counter) | | | |
| H0081 (129) Normal mode | | | |
| H00C1 (193) Precision mode | | | |

| Channel 2 | | | |
|-------------|---------------|-----------|--|
| (| (Slave timer) | | |
| H0011 (17) | 1 kHz | Normal | |
| H0021 (33) | 10 kHz | mode | |
| H0031 (49) | 100 kHz | | |
| H0051 (81) | 1 kHz | Precision | |
| H0061 (97) | 10 kHz | mode | |
| H0071 (113) | 100 kHz | | |

In this mode, channel 2 works relatively with channel 1.

(2) External signals

| Signal | Channel 1 | Channel 2 |
|---------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| Phase A | Counting up pulse | No use |
| Phase B | No use | No use |
| Phase G | Used to enable the operation (enabled while both phase G and soft-gate are ON) | No use |
| Phase M | No use | No use |
| EXT | No use | No use |
| S1 | No use | Hardware comparison output ON when count value > set-point- 1 |
| S2 | No use | No use |

(3) Buffer memory

| Name | Channel 1 | | Channel 2 | | |
|----------------|-----------|-----------------------------------------------------------|-----------|---------------------------------------------------------------|--|
| | Address | Function | Address | Function | |
| Count value | 1.0 | Stores the count value (read/write) | 9.8 | Stores the count value (read/write) | |
| Set-point-1 | 3.2 | Used to set the reset point (read/write) | 11.10 | Used to set the comparison value (read/write) | |
| Set-point-2 | 5.4 | No use | 13.12 | No use | |
| Hold value | 7.6 | Stores the count value at the gate comes OFF (read) | 15.14 | Stores the count value in the CH1 reset interval (read) | |
| Interrupt flag | 16 | Used for interrupt function (read) | 16 | Used for interrupt function (read) | |
| Mode register | 32 | Used to set the operation mode (read/write) | 33 | Used to set the operation mode (read/write) | |

(4) Command register (YW)

| Name | | Channel 1 | Channel 2 | | | | | |
|----------------------|-----|--------------------------------------------------------------------------------------------|-----------|------------------------------------------------------|--|--|--|--|
| | Bit | Function | Bit | Function | | | | |
| Soft-gate | 0 | Used to enable the operation (enabled while both phase G and soft-gate are ON) | 4 | No use | | | | |
| Interrupt- enable | 1 | Set to ON to enable interrupt function for CH1 | 5 | Set to ON to enable interrupt function for CH2 | | | | |
| Output-enable | 2 | No use | 6 | Set to ON to enable hardware comparison output | | | | |

(5) Operation

In this mode, the channel 2 works relatively with the channel 1 operation. The channel 1 is set as the auto-reset universal counter mode. The channel 2 counts the internal clock pulses in the channel 1 reset interval.

When the channel 1 count value reaches the channel 1's set-point-1, the channel 2 count value is transferred into the channel 2's hold register, and both channel 1 and channel 2 count values are reset to 0.

Resulting, the channel 2 measures the time of the channel 1 reset interval.

The frequency of the internal clock can be selected from 1, 10 or 100 kHz. The table below shows the time units which increases the channel 2 count value by 1. The count rage is 1 to 16777215. The countable duration is also shown in the table. If the channel 2 count value exceeds the upper limit value (16777215), it is reset to 0.

| Count mode | Internal clock | Time units (= 1 count) | Countable duration | | | | |
|---------------|----------------|------------------------|-------------------------|--|--|--|--|
| Normal | 1 kHz | 1 ms | 1 ms to 16777.215 s | | | | |
| | 10 kHz | 0.1 ms | 0.1 ms to 1677.7215 s | | | | |
| | 100 kHz | 0.01 ms | 0.01 ms to 167.77215 s | | | | |
| Precision | 1 kHz | 0.5 ms | 0.5 ms to 8388.6075 s | | | | |
| | 10 kHz | 0.05 ms | 0.05 ms to 838.86075 s | | | | |
| | 100 kHz | 0.005 ms | 0.005 ms to 83.886075 s | | | | |

This mode function is enabled while both phase G and soft-gate for channel 1 are ON. (even when the either is OFF, counting is not stopped)

When the channel 2's output-enable bit in the command register (YW) is ON, the hardware comparison output (2S1) is enabled. In this condition, when the channel 2 count value is greater than the channel 2 set-point-1, 2S1 comes ON.

When the channel 2's interrupt-enable bit in the command register (YW) is ON, PI312's interrupt function is enabled. In this condition, when the channel 2 count value reaches the channel 2 set-point-1, the PI312 generates an interrupt signal for the T3.

For details of the channel 1 counter operation, refer to section 6.3 Auto-reset universal counter mode.



(6) Sample program

In the following sample programs, it is assumed that the PI312 is allocated to XW000 and YW001.

• Setting the auto-reset universal counter (normal) for channel 1, and the slave timer (1 kHz, normal) for channel 2

| 1 | |
|---|------------------------------------------|
| | - [88832 HOV RW858]-[88882 MOV RW851]- |
| | - └[D0010 WRITE RW050 → XW000] |

At the beginning of RUN mode (at the first scan), the mode data 129 (H0081) is written into the address 32 (CH1 mode) and the mode data 17 (H0011) is written into the address 33 (CH2 mode) of the buffer memory.

• Reading the status register (XW000) and writing the command register (YW001)

| Channel 1: | Soft-gate (Y0010) = ON |
|------------|--------------------------------|
| | Interrupt-enable (Y0011) = ON |
| | Output-enable (Y0012) = OFF |
| Channel 2: | Soft-gate (Y0014) = OFF |
| | Interrupt-enable (Y0015) = OFF |
| | Output-enable (Y0016) = OFF |
| | |

| | R0100 | | Y9010 |
|---|-------|-------------|-------|
| ì | | | Y0011 |
| 2 | [| (82) XU8887 | |
| 6 | L 170 | (02) M000] | |

When R0100 is ON, Y0010 and Y0011 are set to ON. Then I/O registers (XW000 and YW001) are updated by direct I/O instruction (I/O).

• Writing the set-point data

| C | Channel 1 | Set-point-1 = 3000 |
|---|--------------------|----------------------------------------|
| 1 | R0101 ── | [0000003000 DMOV D0013 D0012] |
| | - | -[88882 MOV RW858]-[88882 MOV RW851] |
| | - | _[D0012 WRITE RW050 → XW000] |

At the rising edge of R0101 coming ON, the data 3000 is written into the addresses 3.2 (CH1 set-point-1).

• Reading the channel 2 hold value in the interrupt program

| 2-(XW888 READ RW868 → RW888] R8888 3 | | 1-[88816 MOV RW868]-[88881 MOV RW861]- |
|--------------------------------------------|-------|---------------------------------------------|
| 3 | _ | 2-(XW000 READ RW060 → RW000) R0000 |
| | | 3 [00014 HOV RW060] [00002 HOV RW061] |
| 4 | RET]- | |

When the channel 1 generates an interrupt, the above interrupt program is executed. In this interrupt program, the interrupt flag (address 16) is read at first. Then the channel 2 hold value (address 15·14) is read and stored in the double-word register D0103·D0102.

Refer to section 7 for more information about the interrupt function.

Section 7

Interrupt Function

- 7.1 Interrupt function
- 7.2 Interrupt control flags
- 7.3 T3 sample program
- 7.4 Precautions on interrupt function

7. Interrupt Function

7.1 Interrupt function

The PI312 has the interrupt function. When an interrupt condition is fulfilled in each operation mode, the PI312 generates an interrupt signal for the T3. Then corresponding I/O interrupt program in the T3 is started immediately. One I/O interrupt program is assigned to one PI312. Therefore, the channel 1 interrupt and the channel 2 interrupt activate the same I/O interrupt program. The interrupt generation condition is explained in section 6 Function Details. This section explains how to use the interrupt function.



The general information about the I/O interrupt program is provided in the T3 User's Manual – Functions.

7.2 Interrupt control flags

To use the interrupt function, set the interrupt-enable flag on the command register YW(n+1) to ON. The bit 1 in the command register is for channel 1 and the bit 5 is for channel 2. Refer to section 4.1 for the bit assignment of the command register.

The PI312's interrupt function is enabled under the condition of both the interruptenable flag and the counter gate (phase G and soft-gate) are ON.

When the T3 receives the interrupt signal from the PI312, the T3 stops other operation, such as main program execution, I/O processing, etc., and immediately starts the corresponding I/O interrupt program execution.

On the I/O interrupt program, read the interrupt flag which is allocated to the address 16 of the PI312's buffer memory by using READ instruction. By reading the interrupt flag, the PI312 recognizes the interrupt acceptance and resets the interrupt flag. If the interrupt flag is not read, the PI312 cannot generate the next interrupt signal.

Interrupt flag (buffer memory)



The source of the interrupt – channel 1 or channel 2 – can also be checked by reading the interrupt flag.

7.3 T3 sample program

An example of the interrupt program is shown below. In this sample program, it is assumed that the PI312 is allocated to XW000 and YW001.

(I/O interrupt #1)



Rung 1 and 2 reads the interrupt flag and stores into RW000.

Rung 3 is for channel 1 interrupt processing. (if interrupt source is channel 1, R0000 comes ON)

Rung 4 is for channel 2 interrupt processing. (if interrupt source is channel 2, R0001 comes ON)

7. Interrupt Function

7.4 Precautions on interrupt function

- The high frequency of the interrupt generation will cause T3 inoperative. Because, in such case, the T3 becomes busy to execute the interrupt program, and cannot execute the main program. It is recommended that the interrupt frequency is 10 ms or more.
- When PI312's interrupt function is used, the interrupt-enable flag and the soft-gate should be controlled (ON or OFF) together.
- If an interrupt signal is generated while T3 is executing other interrupt program, the interrupt signal is held. When the interrupt program execution is finished, the held interrupt signal is accepted by the T3.
- On the T3 program, interrupt enable/disable can be controlled by using El instruction (FUN140) and DI instruction (FUN141). These instructions should be used in a pair in the sequence of DI first and followed by El.



• El and DI instructions should not be used in interrupt program. Also, these instructions should not be executed in the first scan.

Appendix

A.1 Specification of the READ instruction

A.2 Specification of the WRITE instruction

A.3 List of operation mode setting data

Appendix

A.1 Specification of the READ instruction

FUN 237 Special module data read (READ)

Reads designated range of data from the special module.

Execution output \neg A READ B \rightarrow C \neg

Function

Input

- This instruction reads data from the buffer memory of the special module that is designated by operand A, and stores them in T3's registers starting with operand C.
- The transfer source address (buffer memory address) is designated by operand B.
- The transfer size (number of words) is designated by operand B+1.

| Input | Action | Output | ERF |
|-------|--------------------|--------|-----|
| OFF | No execution | OFF | |
| ON | Normal execution | ON | |
| | Error (see Note 2) | ON | ON |

Index

Operand

| | | | | | | | | | | | | | Co | nsta | ant | İ | | | | | | | | | | | | |
|-----|-----------------|---|---|---|---|---|---|----|----|---|---|----|----|------|-----|----|---|---|---|---|---|----|---|---|---|---|--|---|
| | Device Register | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Opr | Name | Х | Υ | S | L | R | Ζ | Т. | C. | Ι | 0 | XW | YW | SW | LW | RW | W | Т | С | D | F | IW | 0 | Ι | J | Κ | | İ |
| | | | | | | | | | | | | | | | | | | | | | | | W | | | | | |
| Α | Special | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | module | | | | | | | | | | | | | | | | | | | | | | | | | | | Ċ |
| В | Transfer | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | parameter | | | | | | | | | | | ` | | ` | ` | | ' | ' | | ` | ' | | | | | | | |
| С | Top register | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | of destination | | | | | | | | | | | | ` | | | , | | | | | - | | | | | | | |

Program example



- When R0000 is ON, the buffer memory data of the size indicated by RW011, starting with the address indicated by RW010 of the special module allocated to XW000, are read and stored in D0100 and after.
- The maximum number of words to be read is 256 words. (17 words for PI312)



Note 1) The special module can be designated not only by the assigned register, but also by the mounting position. The mounting position is designated by a constant data for the operand A as follows.

(Unit number) \times 256 + (Slot number)



| Unit number | Hexadecimal |
|-------------|-------------|
| 0 | H00 |
| 1 | H01 |
| 2 | H02 |
| 3 | H03 |

| Slot number | Hexadecimal |
|-------------|-------------|
| 0 | H00 |
| 1 | H01 |
| 2 | H02 |
| 3 | H03 |
| 4 | H04 |
| 5 | H05 |
| 6 | H06 |
| 7 | H07 |
| 8 | H08 |
| 9 | H09 |
| 10 | H0A |

For example, if a special module is mounted on Slot-4, Unit-0 (basic unit) and allocated to XW008 - YW09, the following two READ instructions function the same.

-----[XW008 READ RW010 \rightarrow D0100]----

-----[H0004 READ RW010 \rightarrow D0100]----

- Note 2) The READ instruction is not executed as error in the following cases. In these cases, ERF (instruction error flag = S0051) is set to ON.
 - When the operand A is other than a valid constant (see Note 1) or XW/YW register.
 - When the designated special module has been disconnected.
 - When no answer error occurs with the designated special module.
 - When the number of words transferred exceeds 256 words.
 - When the source table of transfer is out of the valid range.
 - When the destination table of transfer is out of the valid range.

Appendix

A.2 Specification of the WRITE instruction

FUN 238 Special module data write (WRITE)

Writes designated range of data into the special module.

Input [A WRITE B \rightarrow C]-

Execution output

Function

- This instruction transfers data stored in T3's registers starting with operand A into the buffer memory of the special module that is designated by operand C.
- The destination address (buffer memory address) is designated by operand B.
- The transfer size (number of words) is designated by operand B+1.

| Input | Action | Output | ERF |
|-------|--------------------|--------|-----|
| OFF | No execution | OFF | |
| ON | Normal execution | ON | |
| | Error (see Note 2) | ON | ON |

Index

Operand

| | | Constant | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|---------------------------|----------|---|---|---|---|---|----|----------|---|---|----|----|----|----|----|--------------|---|---|---|---|----|----|---|---|---|--------------|--------------|
| | | Device | | | | | | | Register | | | | | | | | | | | | | | | | | | | |
| Opr | Name | Х | Y | S | L | R | Ζ | Τ. | C. | Ι | 0 | XW | YW | SW | LW | RW | W | Т | С | D | F | IW | 0 | Ι | J | К | | |
| A | Top register of source | | | | | | | | | | | | | | | | \checkmark | | | | | | ~~ | | | | | \checkmark |
| В | Transfer parameter | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| С | Special module | | | | | | | | | | | | | | | | | | | | | | | | | | \checkmark | |

Program example



- When R0000 is ON, the register data of the size indicated by RW011, starting with D0100, are transferred to the buffer memory starting with the address indicated by RW010 of the special module allocated to YW001.
- The maximum number of words to be transferred is 256 words. (6 words for PI312)



Note 1) The special module can be designated not only by the assigned register, but also by the mounting position. The mounting position is designated by a constant data for the operand C as follows.

(Unit number) \times 256 + (Slot number)



| Unit number | Hexadecimal | | | | | |
|-------------|-------------|--|--|--|--|--|
| 0 | H00 | | | | | |
| 1 | H01 | | | | | |
| 2 | H02 | | | | | |
| 3 | H03 | | | | | |
| | | | | | | |

| Slot number | Hexadecimal | | | | | | |
|-------------|-------------|--|--|--|--|--|--|
| 0 | H00 | | | | | | |
| 1 | H01 | | | | | | |
| 2 | H02 | | | | | | |
| 3 | H03 | | | | | | |
| 4 | H04 | | | | | | |
| 5 | H05 | | | | | | |
| 6 | H06 | | | | | | |
| 7 | H07 | | | | | | |
| 8 | H08 | | | | | | |
| 9 | H09 | | | | | | |
| 10 | H0A | | | | | | |

For example, if a special module is mounted on Slot-2, Unit-1 (expansion unit #1) and allocated to XW020 - YW021, the following two WRITE instructions function the same.

-----[D0100 WRITE RW010 \rightarrow XW020]-----

-----[D0100 WRITE RW010 \rightarrow H0102]-----

- Note 2) The WRITE instruction is not executed as error in the following cases. In these cases, ERF (instruction error flag = S0051) is set to ON.
 - When the operand C is other than a valid constant (see Note 1) or XW/YW register.
 - When the designated special module has been disconnected.
 - When no answer error occurs with the designated special module.
 - When the number of words transferred exceeds 256 words.
 - When the source table of transfer is out of the valid range.
 - When the destination table of transfer is out of the valid range.

Appendix

A.3 List of operation mode setting data

| Operation | n mode | Pulse count | Internal clock | Opera | Jumper | | |
|-------------------|---------------|-------------|----------------|-------|--------|-----------|--|
| | | mode | selection | mode | | piug (JZ) | |
| Quadrature bi-p | uise counter | Normal | No use | H0002 | (2) | Short | |
| mode | | Precision | No use | H0042 | (66) | | |
| Up/down pulse of | counter mode | Normal | No use | H0000 | (0) | Short | |
| | | Precision | No use | H0040 | (64) | | |
| Auto-reset unive | ersal counter | Normal | No use | H0081 | (129) | Short | |
| mode | | Precision | No use | H00C1 | (193) | | |
| Universal counter | er mode | Normal | No use | H0001 | (1) | Short | |
| | | Precision | No use | H0041 | (65) | | |
| Speed counter | 0.01 | Normal | No use | H0005 | (5) | Short | |
| | second | | | | | | |
| mode | sampling | Precision | No use | H0045 | (69) | | |
| | 0.1 second | Normal | No use | H000D | (13) | | |
| | sampling | Precision | No use | H004D | (77) | | |
| Programmable i | nterval timer | Normal | 1 kHz | H0091 | (145) | Short | |
| mode | | | 10 kHz | H00A1 | (161) | | |
| | | | 100 kHz | H00B1 | (177) | | |
| | | Precision | 1 kHz | H00D1 | (209) | | |
| | | | 10 kHz | H00E1 | (225) | | |
| | | | 100 kHz | H00F1 | (241) | | |
| Gate-ON timer n | node | Normal | 1 kHz | H0011 | (17) | Short | |
| | | | 10 kHz | H0021 | (33) | | |
| | | | 100 kHz | H0031 | (49) | | |
| | | Precision | 1 kHz | H0051 | (81) | | |
| | | | 10 kHz | H0061 | (97) | | |
| | | | 100 kHz | H0071 | (113) | | |
| Slave counter m | ode | Normal | No use | H0001 | (1) | Open | |
| | | Precision | No use | H0041 | (65) | | |
| Slave timer mod | e | Normal | 1 kHz | H0011 | (17) | Open | |
| | • | | 10 kHz | H0021 | (33) | | |
| | | | 100 kHz | H0031 | (49) | | |
| | | Precision | 1 kHz | H0051 | (81) | | |
| | | | 10 kHz | H0061 | (97) | | |
| | | | 100 kHz | H0071 | (113) | | |

Note) The number in brackets () on the operation mode data column shows the decimal value of the operation mode data.

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