TOSHIBA

UM-TS02∗∗∗-E021

PROGRAMMABLE CONTROLLER

PROSEC **T2-series**

PULSE INPUT MODULE

PI232/PI272

USER'S MANUAL

TOSHIBA CORPORATION

Important Information

Misuse of this equipment can result in property damage or human injury.
Because controlled system applications vary widely, you should satisfy yourself as to the acceptability of this equipment for your intended purpose.
In no event will Toshiba Corporation be responsible or liable for either indirect or consequential damage or injury that may result from the use of this equipment.

No patent liability is assumed by Toshiba Corporation with respect to use of information, illustrations, circuits, equipment or examples of application in this publication.

Toshiba Corporation reserves the right to make changes and improvements to this publication and/or related products at any time without notice. No obligation shall be incurred other than as noted in this publication.

Publication number: UM-TS02***-E021
1st edition September 1999

Safety Precautions

This module PI232/PI272 is a pulse input module for Toshiba's Programmable Controller PROSEC T2-series (T2/T2E/T2N).
Read this manual thoroughly before using this module. Also, keep this manual and related manuals so that you can read them anytime while this module is in operation.

Safety Symbols

The following safety symbols are used on the product and/or in the related manuals.
Pay attention to information preceded by the following symbols for safety.

⚠ WARNING — Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

⚠ CAUTION — Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury. It may also be used to alert against unsafe practices.

Safety Precautions

⚠ CAUTION

- Turn off power to the PLC (T2, T2E or T2N) and to this module (PI232/PI272) before removing or mounting this module. Failure to do so can cause electrical shock or damage to this product.
- Read the Safety Precautions described in the T2, T2E or T2N User's Manual before using this module.
- Follow the instructions described in this manual and in the T2, T2E or T2N User's Manual when installing and wiring this module.
- This module has been designed for the T2/T2E/T2N. Use your PI232/PI272 only on the T2-series PLC rack.
- Remove this module from the rack before setting the DIP switches on this module. Do not touch other components on this module's printed circuit board. It may cause damage to this module.
- This module consumes maximum 500 mA (PI232) or 650 mA (PI272) of internal 5 Vdc power. Confirm that the total 5 Vdc consumed current per one power supply module is within the limit (2.5 A).
  If it exceeds the limit, the T2/T2E/T2N cannot operate properly and this may cause unsafe situation.

About This Manual

About This Manual

This manual explains the specifications and operations of the Pulse Input Module PI232 and PI272 for Programmable Controller T2-series. Read this manual carefully before using the PI232 or PI272.
In this manual, PI232 and PI272 are called as "PI232/272" for explaining common functions of these modules. The T2-series Programmable Controllers, T2, T2E or T2N, are called as "T2" in this manual.

Inside This Manual

Section 1 Overview
This section introduces the PI232/272. The PI232/272 has seven (7) operation modes. This section outlines the PI232/272's operation modes. Read this section at first to get basic understanding of the operation modes and to decide the operation mode for your intended application.

Section 2 Specifications
This section provides the hardware and functional specifications of the PI232/272. Refer to this section to check applicability of the PI232/272 with your intended system.

Section 3 Wiring
This section provides the information for external wire connections. Depending on the operation modes, wire connections are different. Read this section after you have decided the operation mode. Wiring precautions are also provided in this section.

Section 4 Register Configuration
This section provides the information to design T2 program for the PI232/272. This section explains the I/O allocation and functions of the I/O registers assigned to the PI232/272. Also, this section explains the buffer memory contents that is provided in the PI232/272, and how to access the buffer memory by T2 program.

Section 5 Operation Mode Setting
This section explains the method for setting the PI232/272 to your desired operation mode. The PI232/272's operation mode is determined by setting the DIP switches on the PI232/272 and by writing a mode data into the PI232/272's buffer memory. T2 sample programs for setting the PI232/272's operation mode are provided in this section.

Section 6 Function Details
This section explains details of each operation mode. This section consists in seven (7) clauses according to the operation modes. Each clause contains the explanation for functions, necessary external signals, I/O register and buffer memory usage, and T2 sample programs. Read the clause for your intended operation mode.

Appendix
The specifications of READ and WRITE instructions are described. These instructions are used for interchanging data between T2 and PI232/272.

Related Manuals

The following related manuals are available. Besides this manual, read the following manuals for your better understanding.

T2E User's Manual
This manual covers the T2E's hardware (main body and basic I/O) - their specifications, handling, maintenance and services. It also explains the functions of the T2E and how to use them. The necessary information to create user program is covered in this manual.

T2N User's Manual
This manual covers the T2N's hardware (main body and basic I/O) - their specifications, handling, maintenance and services. It also explains the functions of the T2N and how to use them. The necessary information to create user program is covered in this manual.

T2 User's Manual
This manual covers the T2's hardware (main body and basic I/O) - their specifications, handling, maintenance and services. It also explains the functions of the T2 and how to use them. The necessary information to create user program is covered in this manual.

T-series Instruction Set
This manual provides the detailed specifications of instructions for Toshiba's T-series Programmable Controllers.

T-PDS for Windows Operation Manual
T-series program development system (T-PDS for Windows) is a programming software for T-series programmable controllers. This manual explains the functions and operations of the T-PDS for Windows.

T-series Handy Programmer (HP911) Operation Manual
This manual explains the functions and key operations of the T-series Handy Programmer (HP911).

Other than the listed above, some T2 related manuals for special I/O modules and data transmission modules are available. Contact Toshiba for more information.

Contents

Section 1

PI232/272 Overview

1. PI232/272 Overview

1.1 Introduction

The pulse input module PI232/272 is a high-speed pulse counter module for Toshiba's Programmable Controller T2.
The PI232/272 has 2 channels of pulse inputs, channel 1 (CH1) and channel 2 (CH2), and can count up to 100 kpps pulses individually for each channel. (max. 50 kpps in quadrature bi-pulse counter mode)

The PI232 and PI272 are different in the pulse input circuits as follows.

PI232	Voltage input	5 Vdc, 12 Vdc, or 24 Vdc
PI272	Line receiver input	Conform to RS-422-A

Except the pulse input circuit, there is no functional difference between PI232 and PI272.

The PI232/272 has total 7 operation modes as listed below.

(1) Quadrature bi-pulse counter mode
(2) Up/down pulse counter mode
(3) Auto-reset universal counter mode
(4) Universal counter mode
(5) Speed counter mode
(6) Programmable interval timer mode
(7) Gate-ON timer mode

In the above (1) through (5) modes, the PI232/272 counts external pulses. In the (6) and (7) modes, the PI232/272 counts its internal clock pulses, resulting it functions as timer. These (1) through (7) modes can be set individually for channel 1 and channel 2.

User can set the operation mode of the PI232/272. Refer to section 5.
The function of each operation mode is outlined in section 1.2, and explained in detail in section 6.

The PI232/272 can be applied for wide range of applications by selecting the operation mode.

NOTE

(1) Proper mode setting is important to use the PI232/272. If it has not set correctly, the PI232/272 will not work as expected.
(2) The maximum number of PI232/272s that can be used with one T2 is not limited by software. However, the PI232 consumes maximum 500 mA of internal 5 Vdc power, and the PI272 consumes maximum 650 mA of internal 5 Vdc power. Confirm that the total 5 Vdc consumed current per one power supply module is within the limit (2.5 A). Refer to the T2/T2E/T2N User's Manual.

1.2 Operation mode overview

This section outlines the PI232/272's operation modes. Read this section to get basic understanding of the operation modes.

1.2.1 Counter operation mode

(1) Quadrature bi-pulse counter mode

PI232/272 counts the pulses whose phases are shifted 90° each other. When phase A pulse precedes against phase B pulse, the PI232/272 counts up (increase). On the other hand, when phase B pulse precedes, the PI232/272 counts down (decrease).

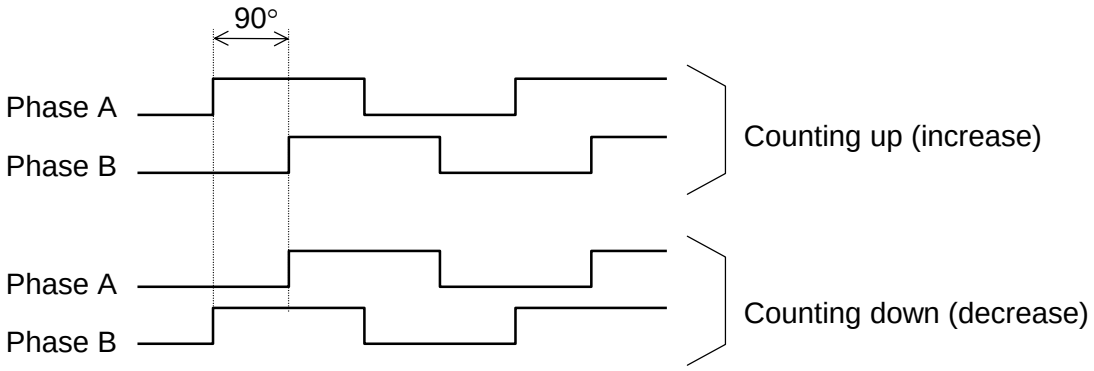
The counter works as a ring counter with the data range of 0 to 16777215.
When the count value is increased by 1 in the upper limit value (16777215), it is reset to 0. When the count value is decreased by 1 in the lower limit value (0), it is reset to the upper limit value (16777215).

Two points of comparison values can be set. These are called "set-point-1" and "set-point-2".
When the count value is greater than the set-point-1, the PI232/272's hardware comparison output (∗S1) comes ON. When the count value is smaller than the set-point-2, the PI232/272's hardware comparison output (∗S2) comes ON.

Note) The asterisk (∗) in the above paragraph represents 1 or 2. 1S1 and 1S2 are the outputs for channel 1, and 2S1 and 2S2 are the outputs for channel 2.

The count value is stored in the PI232/272's buffer memory. This value can be read or written (preset) by T2 with the READ instruction (FUN237) or the WRITE instruction (FUN238), as well as the set-point-1 and set-point-2.

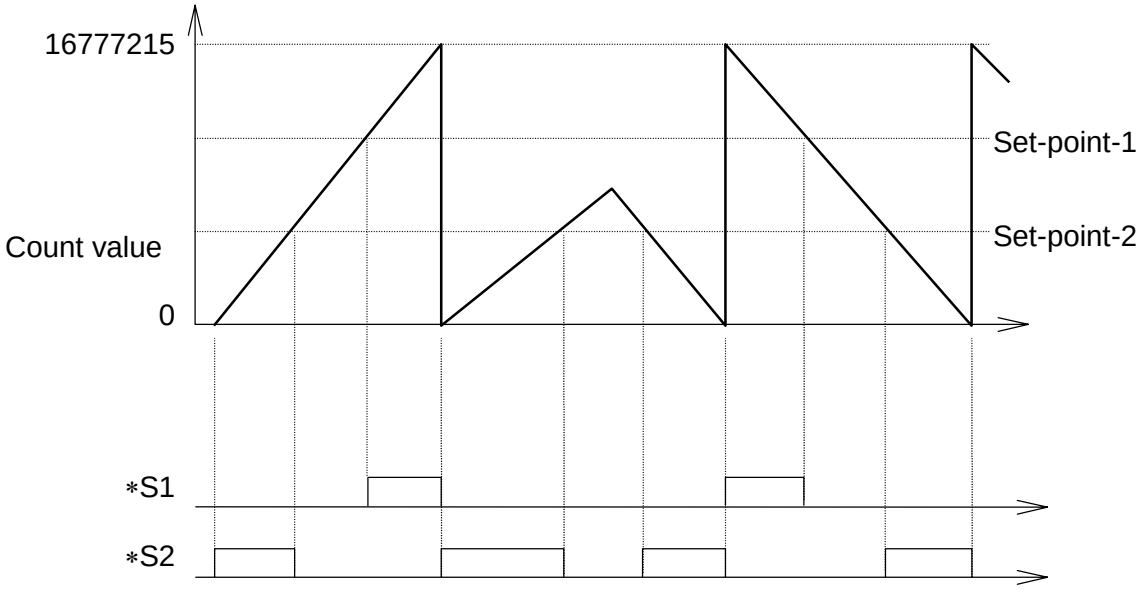
Pulse form (time chart)



NOTE

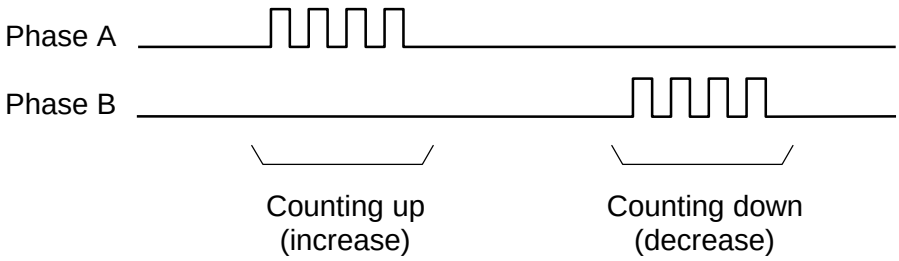
User can exchange the function of phases A and B. The above time-chart shows the default condition. For this setting, refer to section 5.

Counter operation



(2) Up/down pulse counter mode

PI232/272 counts up (increase) by the pulses into phase A, and counts down (decrease) by the pulses into phase B.



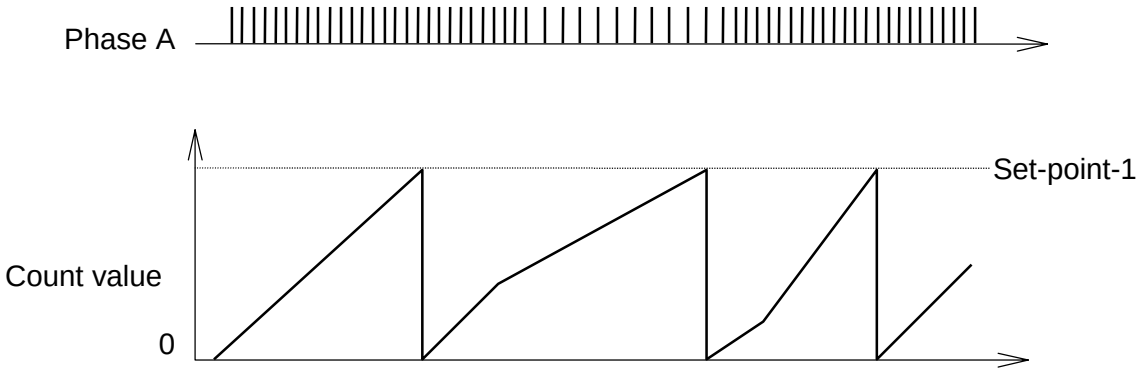
All other functions are the same as that of (1) Quadrature bi-pulse counter mode.

NOTE

User can exchange the function of phases A and B. The above time-chart shows the default condition. For this setting, refer to section 5.

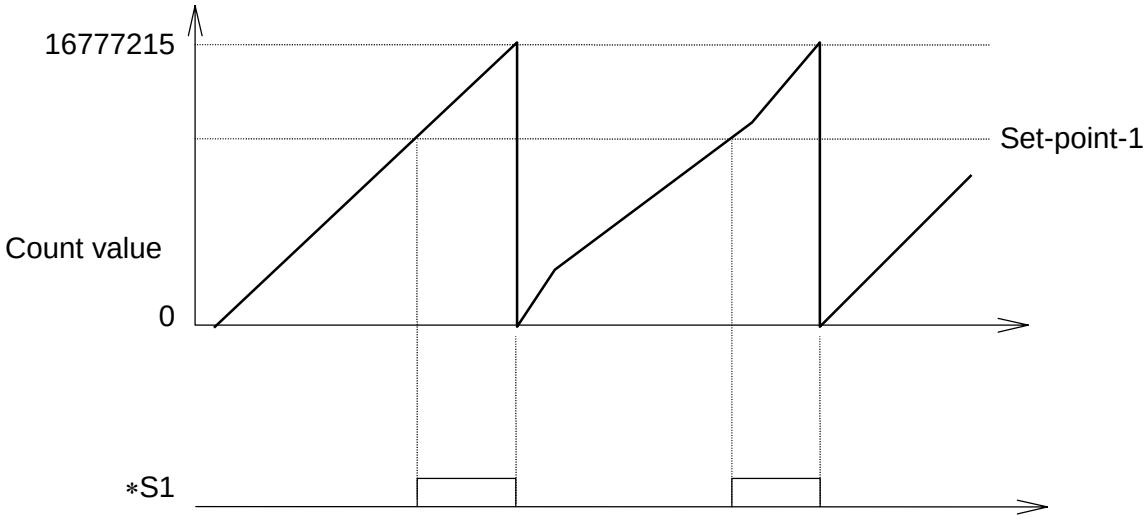
(3) Auto-reset universal counter mode

PI232/272 counts up by the single phase pulses into phase A.
When the count value reaches the set-point-1, the count value is reset to 0 (zero).
The set-point-1 can be set in the range of 1 to 16777215.



(4) Universal counter mode

PI232/272 counts up by the single phase pulses into phase A.
Different from the (3) Auto-reset universal counter mode, the counting continues until the upper limit value (16777215). When the count value exceeds the upper limit value, it is reset to 0 (zero).
PI232/272's comparison output for the set-point-1 (∗S1) can be used.

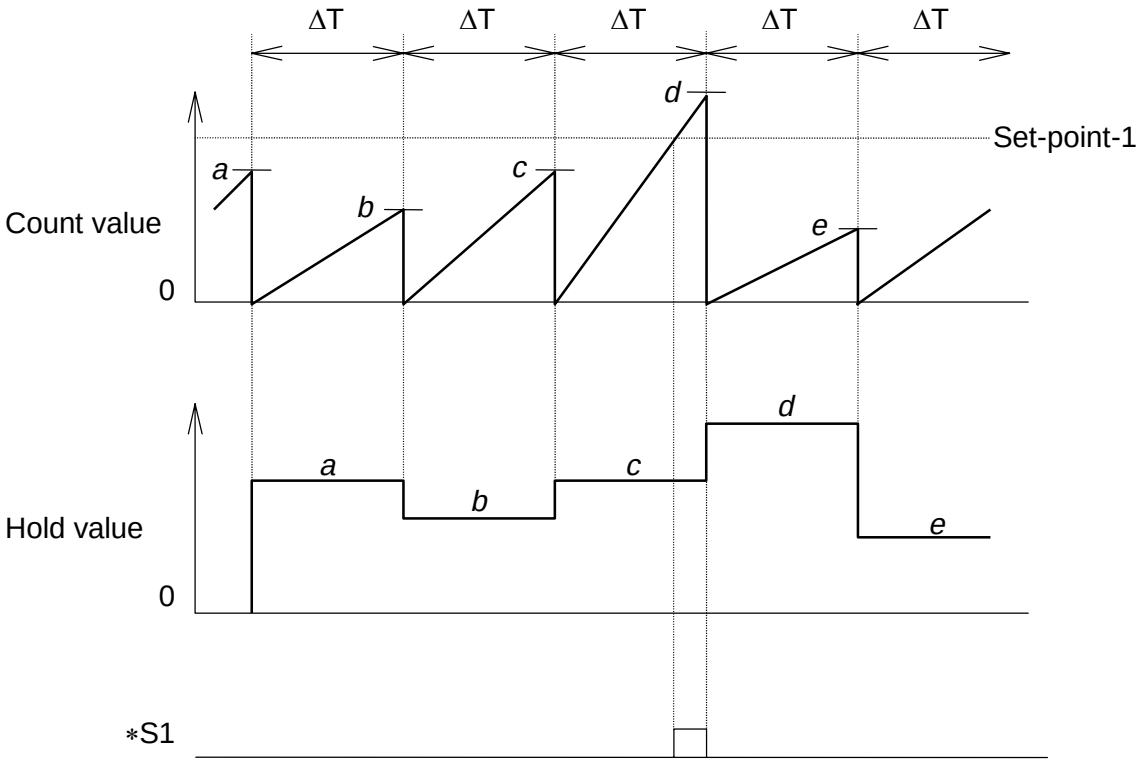


(5) Speed counter mode

PI232/272 counts the single phase pulses into phase A during the specified sampling time.
Then the PI232/272 transfers the count value in a sampling time into the hold register that is allocated on the PI232/272's buffer memory.

By using this mode, the frequency of the pulses can be measured.

The sampling time can be selected from 0.01, 0.1, or 1 second.
PI232/272's comparison output for the set-point-1 (∗S1) can be used.

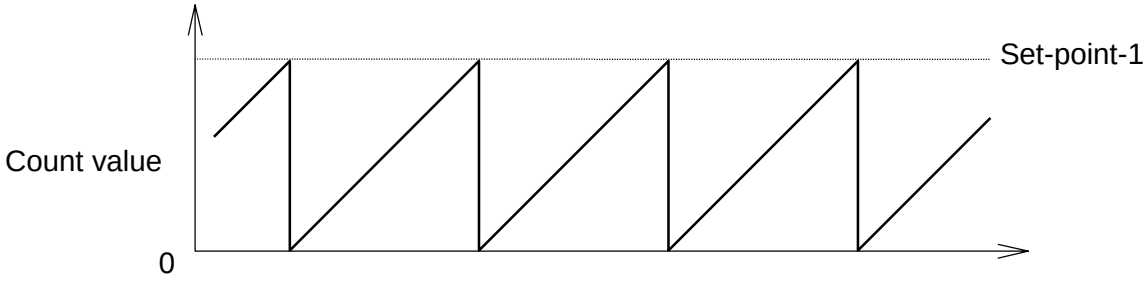


ΔT: sampling time = 0.01s, 0.1s, or 1 s

(6) Programmable interval timer mode

Instead of external pulses, PI232/272 counts its internal clock pulses. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.
All other functions are the same as that of (3) Auto-reset universal counter mode.

In this mode, the PI232/272 works as free-running timer. By using this mode, precise time base control (1 ms, 0.1 ms or 0.01 ms units) is possible.

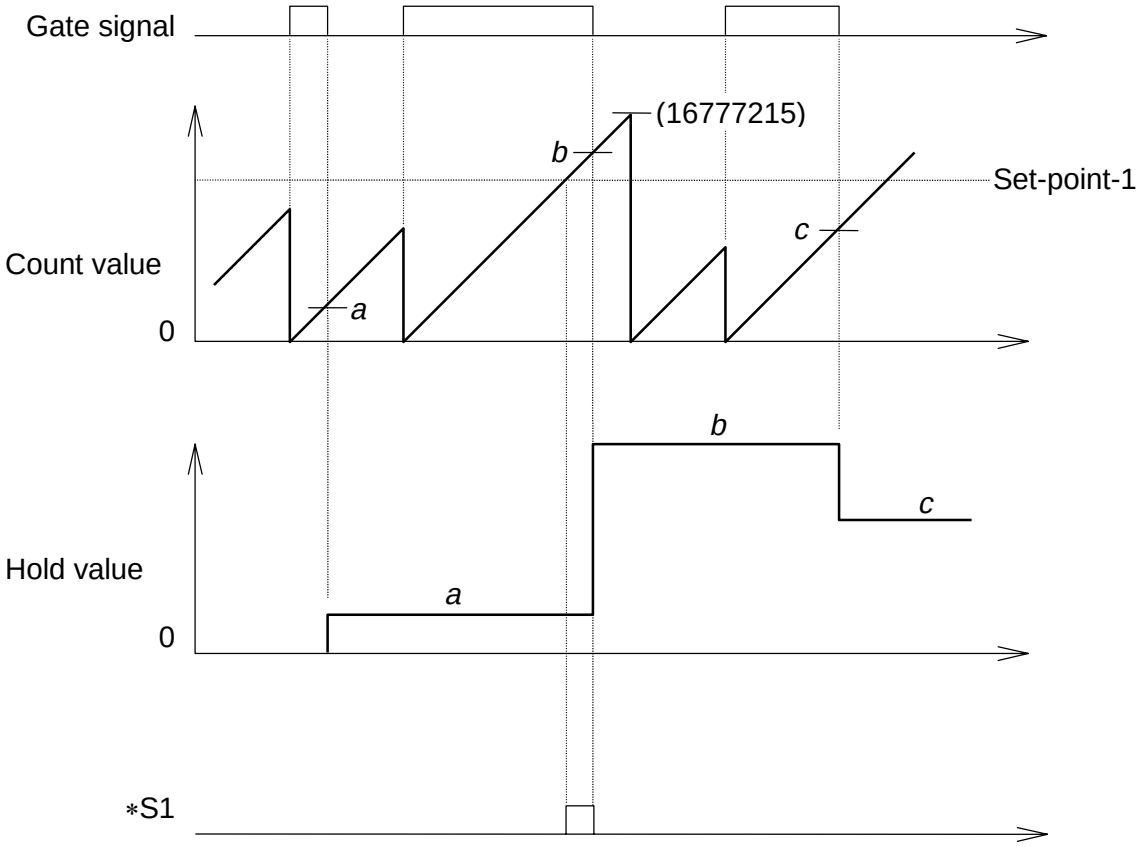


(7) Gate-ON timer mode

PI232/272 functions to measure the ON duration of the external Gate signal.
The time is measured by PI232/272's internal clock. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

When the Gate signal is changed form OFF to ON, the PI232/272 resets the count value. Then when the signal is changed from ON to OFF, the PI232/272 transfers the count value into the hold register that is allocated on the PI232/272's buffer memory.

PI232/272's comparison output for the set-point-1 (∗S1) can be used.

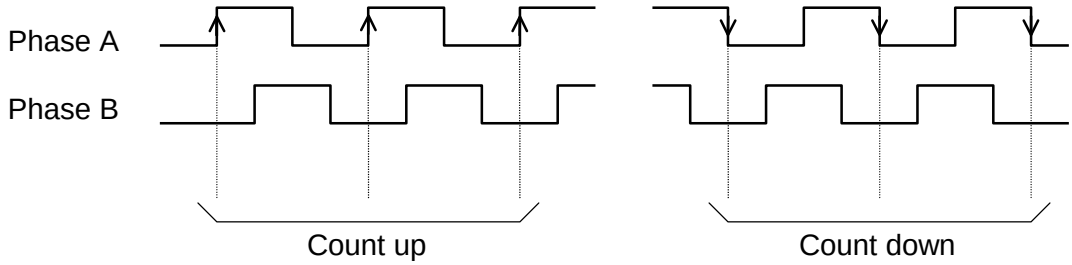


1.2.2 Pulse count mode

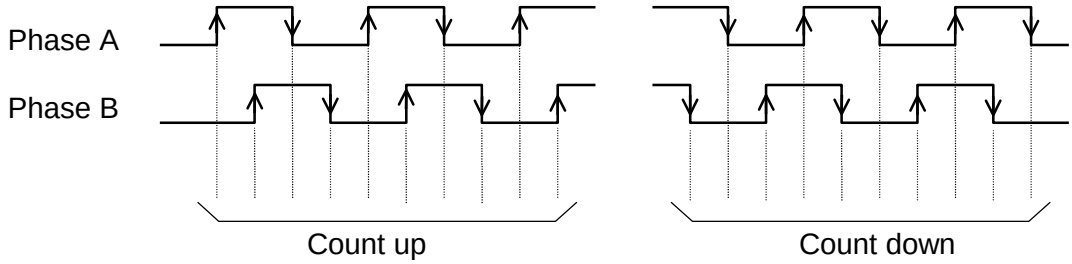
The PI232/272 has 2 modes for pulse counting. They are the normal count mode and the precision count mode.
In the normal count mode, the PI232/272 counts at either rising or falling edge of the pulse. On the other hand, in the precision count mode, the PI232/272 counts at both rising and falling edges. See the timing diagram below.
The pulse count mode can be selected individually for channel 1 and channel 2.

Quadrature bi-pulse counter mode:

<Normal count mode>

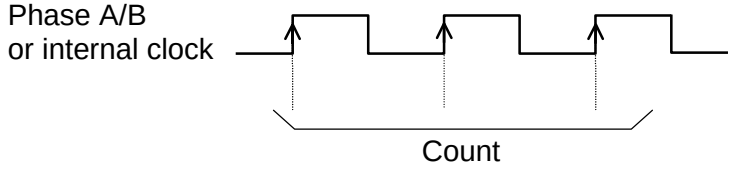


<Precision count mode>

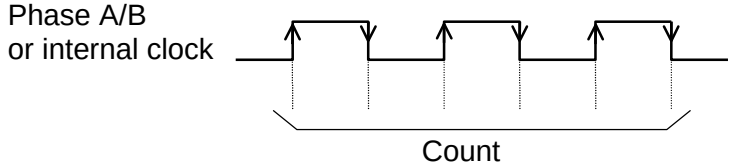


Other than the quadrature bi-pulse counter mode:

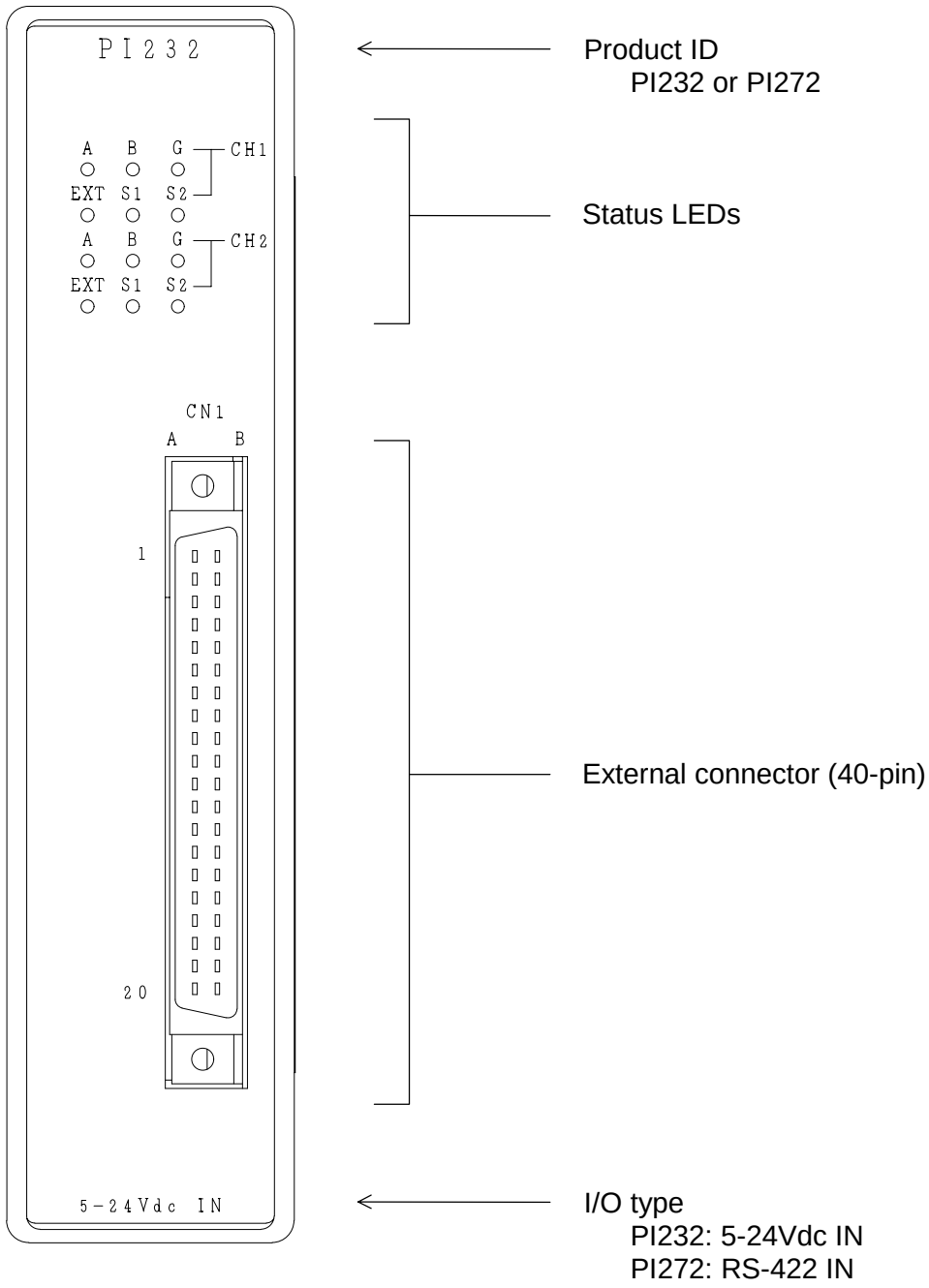
<Normal count mode>



<Precision count mode>



1.3 External features



NOTE The cable side connector (soldering type) is standard accessory.

Status LEDs

Indicates the PI232/272 operation status. Six LEDs are provided for each channel.

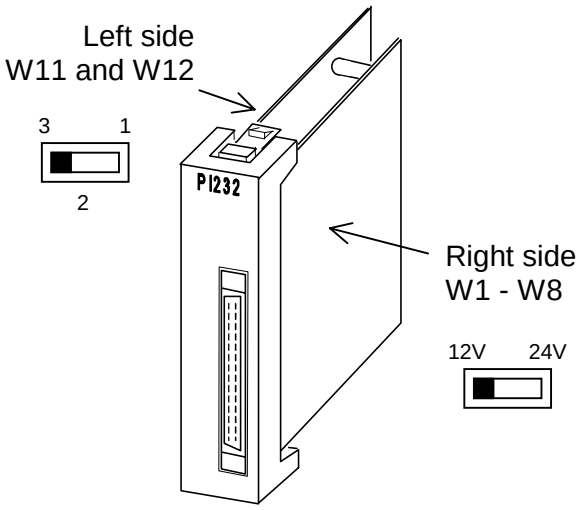
A	Lit when the phase A pulse input is ON (see Note 1)
B	Lit when the phase B pulse input is ON
G	Lit when both the gate input and the soft-gate are ON (see Note 2)
EXT	Lit when the external limit input (EXT) is ON
S1	Lit when the comparison output (∗S1) is ON
S2	Lit when the comparison output (∗S2) is ON

NOTE

(1) In the programmable interval timer and the gate ON timer modes, this LED is controlled by the internal clock.
(2) For the soft-gate, refer to section 4.1.

DIP switches

The DIP switches W1 to W8 are provided only on the PI232 to select the input voltage either 12 or 24 Vdc. For 5 Vdc input, it is selected by connection terminal. Refer to section 3.
The DIP switches W11 and W12 are provided on both the PI232 and the PI272. The W11 is used to select the timing of PI232/272's internal memory initialization.



Input voltage setting (PI232 only)

	Function	Setting	
		12V-side	24V-side
W1	CH1 phase A	12 Vdc	24 Vdc
W2	CH1 phase B	12 Vdc	24 Vdc
W3	CH1 marker	12 Vdc	24 Vdc
W4	CH2 phase A	12 Vdc	24 Vdc
W5	CH2 phase B	12 Vdc	24 Vdc
W6	CH2 marker	12 Vdc	24 Vdc
W7	CH1 gate input	12 Vdc	24 Vdc
W8	CH2 gate input	12 Vdc	24 Vdc

Function setting (both PI232 and PI272)

	Setting	Function
W11	3-side	Initialized at both power-on and RUN mode transition
	1-side	Not initialized at RUN mode transition
W12	3-side	No use (fix to 3-side)
	1-side	

NOTE

Factory setting is 12V-side for W1 to W8, and 3-side for W11 and W12.
Use tweezers or equivalent to change the settings.

External connector

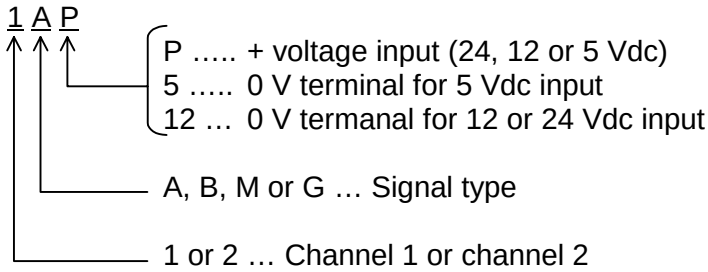
One 40-pin connector (female) is provided for connecting the external signals.

< PI232 >

Function	Name	Pin No. A	Pin No. B	Name	Function
Channel 1 Phase A input	1A5	1	1	1AP	Channel 1 Phase A input
Channel 1 Phase B input	1BP	2	2	1A12	
	1B12	3	3	1B5	Channel 1 Phase B input
Channel 1 Maker input	1MP	4	4	1M5	Channel 1 Maker input
	1M12	5	5	2AP	Channel 2 Phase A input
Channel 2 Phase A input	2A5	6	6	2A12	
Channel 2 Phase B input	2BP	7	7	2B5	Channel 2 Phase B input
	2B12	8	8	2MP	Channel 2 Maker input
Channel 2 Maker input	2M5	9	9	2M12	
Channel 1 Gate input	1GP	10	10	1G5	Channel 1 Gate input
	1G12	11	11	2GP	Channel 2 Gate input
Channel 2 Gate input	2G5	12	12	2G12	
Channel 1 External limit input	1EXT-	13	13	1EXT+	Channel 1 External limit input
Channel 2 External limit input	2EXT-	14	14	2EXT+	Channel 2 External limit input
Channel 1 Compare output 2	1S2	15	15	1S1	Channel 1 Compare output 1
Channel 2 Compare output 2	2S2	16	16	2S1	Channel 2 Compare output 1
No use		17	17		No use
24 Vdc input	P24	18	18	P24	24 Vdc input
0 V for compare outputs	N24	19	19	N24	0 V for compare outputs
No use		20	20		No use

Remarks:

For phase A, B, zero maker and gate input, the signal name means as follows.



NOTE

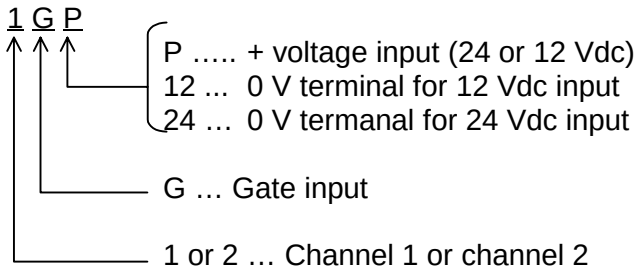
(1) Internal circuit for phase A, B, M, G and EXT input are isolated each other.
(2) For external wiring, refer to section 3.

< PI272 >

Function	Name	Pin No. A	Pin No. B	Name	Function
Channel 1 Phase A +	1A+	1	1	1A–	Channel 1 Phase A –
Channel 1 Phase B +	1B+	2	2	1B–	Channel 1 Phase B –
Channel 1 Maker +	1M+	3	3	1M–	Channel 1 Maker –
Channel 2 Phase A +	2A+	4	4	2A–	Channel 2 Phase A –
Channel 2 Phase B +	2B+	5	5	2B–	Channel 2 Phase B –
Channel 2 Maker +	2M+	6	6	2M–	Channel 2 Maker –
Line receiver signal ground	SG	7	7	SG	Line receiver signal ground
Channel 1 Gate input	1G24	8	8	1G12	Channel 1 Gate input
	1GP	9	9	2GP	Channel 2 Gate input
Channel 2 Gate input	2G12	10	10	2G24	
No use		11	11		No use
Channel 1 Extermal limit input	1EXT-	12	12	1EXT+	Channel 1 External limit input
Channel 2 External limit input	2EXT-	13	13	2EXT+	Channel 2 External limit input
No use		14	14		No use
Channel 1 Compare output 2	1S2	15	15	1S1	Channel 1 Compare output 1
Channel 2 Compare output 2	2S2	16	16	2S1	Channel 2 Compare output 1
No use		17	17		No use
24 Vdc input	P24	18	18	P24	24 Vdc input
0 V for compare outputs	N24	19	19	N24	0 V for compare outputs
No use		20	20		No use

Remarks:

For gate input, the signal name means as follows.



NOTE

(1) Phase A, B and M inputs conform to EIA RS-422-A. (Am26LS31 or equivalent)
(2) For external wiring, refer to section 3.

1. PI232/272 Overview

Section 2

Specifications

2. Specifications

2.1 General specifications

Item	PI232	PI272	Remarks
Power voltage	5 Vdc (supplied from back plane bus)		
Current consumption	Max. 500 mA (5 Vdc)	Max. 650 mA (5 Vdc)	Note (1)
Environmental conditions	Conforms to T2 specifications		
Insulation resistance	10 MΩ (500 Vdc)		Note (2)
Withstand voltage	1500 Vac - 1 minute	500 Vac - 1 minute	Note (2)
Size	T2 I/O module size (1 slot)		
Weight	250 g		

Note (1) The T2's power supply module can supply maximum 2.5 A of internal 5 Vdc. Check that the internal 5 Vdc current consumption per one power supply module does not exceed the limit.

Note (2) Between external and internal circuits.

2.2 Functional specifications

Item	Specifications
Module type	Pulse input
I/O allocation type	X+Y 2W
Number of pulse input channels	2 channels
Counter configuration	24-bit, binary counter Count value = 0 to 16777215
Input pulse frequency	100 kpps maximum (other than quadrature bi-pulse) 50 kpps maximum (quadrature bi-pulse)
Counter operation mode	• Quadrature bi-pulse counter • Up/down pulse counter • Auto-reset universal counter • Universal counter • Speed counter • Programmable interval timer • Gate-ON timer
Pulse count mode	• Normal mode (1 count per 1 pulse) • Precision count mode (both rising and falling edges)
Hardware comparison output function	2 points for each channel (transistor outputs) ∗S1: ON when Count value > set-point-1 ∗S2: ON when Count value < set-point-2
Other functions	• External gate force ON • Phases A and B function exchange • Count disable

2.3 Input/output specifications

- **Input**

< PI232 >

Item		Specifications		
Phase A Phase B Maker Gate	Input voltage	5 Vdc, ±5%	12 Vdc, ±5%	24 Vdc, ±5%
	Input current	15.5 mA	15 mA	12.5 mA
	Minimum ON voltage	3.75 V	9.5 V	21 V
	Maximum OFF voltage	1.25 V	2.5 V	5 V
	Pulse duration (ON level/OFF level)	5 μs or more (other than quadrature bi-pulse) 10 μs or more (quadrature bi-pulse)		
	ON/OFF transition	1.5 μs or less (other than quadrature bi-pulse) 3 μs or less (quadrature bi-pulse)		
EXT	Input voltage	12 - 24 Vdc, +10%/-15%		
	Input current	10 mA (24 Vdc)		
	Minimum ON voltage	9.6 V		
	Maximum OFF voltage	3.5 V		
	ON delay	10 ms or less		
	OFF delay	15 ms or less		

< PI272 >

Item		Specifications	
Phase A Phase B Maker	Electrical specifications	Conform to EIA RS-422-A (Line receiver: Am26LS31 or equivalent)	
	Pulse duration (ON level/OFF level)	5 μs or more (other than quadrature bi-pulse) 10 μs or more (quadrature bi-pulse)	
	ON/OFF transition	1.5 μs or less (other than quadrature bi-pulse) 3 μs or less (quadrature bi-pulse)	
Gate	Input voltage	12 Vdc, ±5%	24 Vdc, ±5%
	Input current	15 mA	12.5 mA
	Minimum ON voltage	9.5 V	21 V
	Maximum OFF voltage	2.5 V	5 V
EXT	Input voltage	12 - 24 Vdc, +10%/-15%	
	Input current	10 mA (24 Vdc)	
	Minimum ON voltage	9.6 V	
	Maximum OFF voltage	3.5 V	
	ON delay	10 ms or less	
	OFF delay	15 ms or less	

2. Specifications

- **Output**

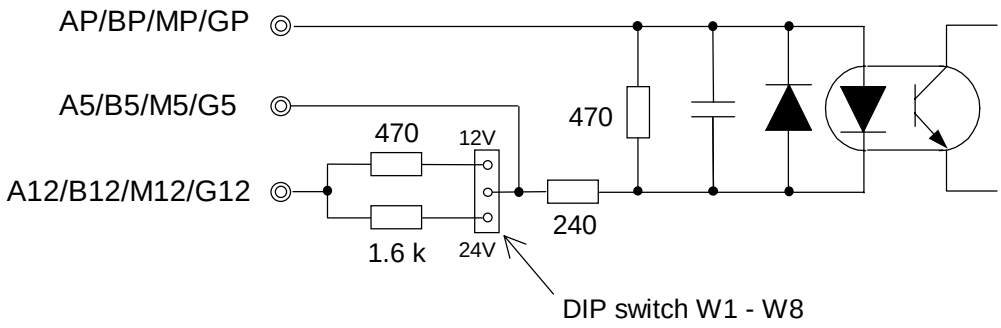
  < PI232/PI272 >

Item		Specifications
1S1 1S2 2S1 2S2	Output method	Transistor output (current sinking)
	Output voltage	10 - 30 Vdc
	Output current	100 mA or less
	Voltage drop at ON	1.0 V or less
	Leakage current at OFF	0.1 mA or less
	ON delay	1 ms or less
	OFF delay	1 ms or less

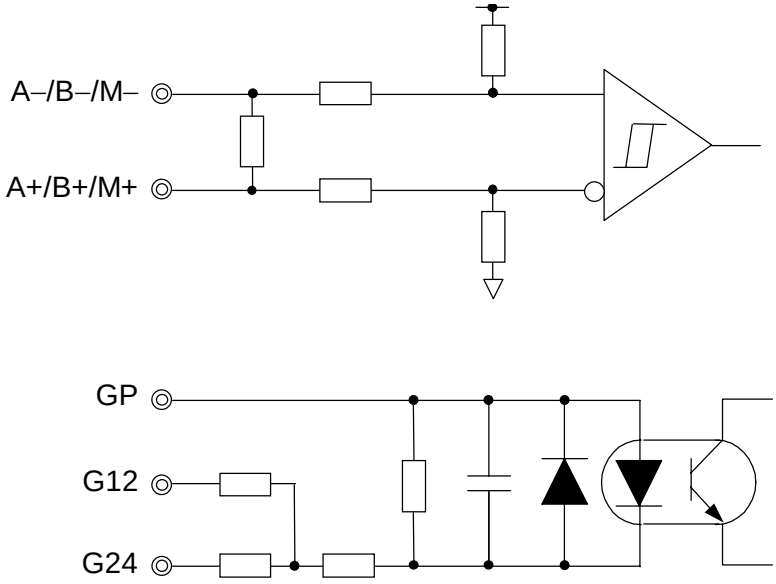
2.4 Input/output internal circuit

- **Pulse input circuit (phase A, B, Maker, Gate)**

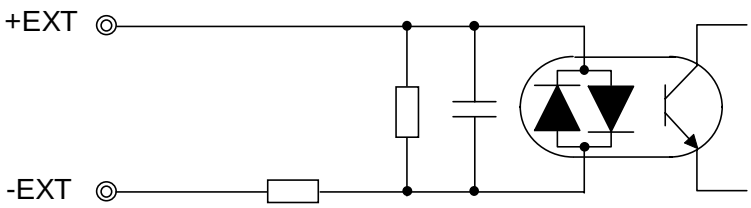
  < PI232 >



  < PI272 >

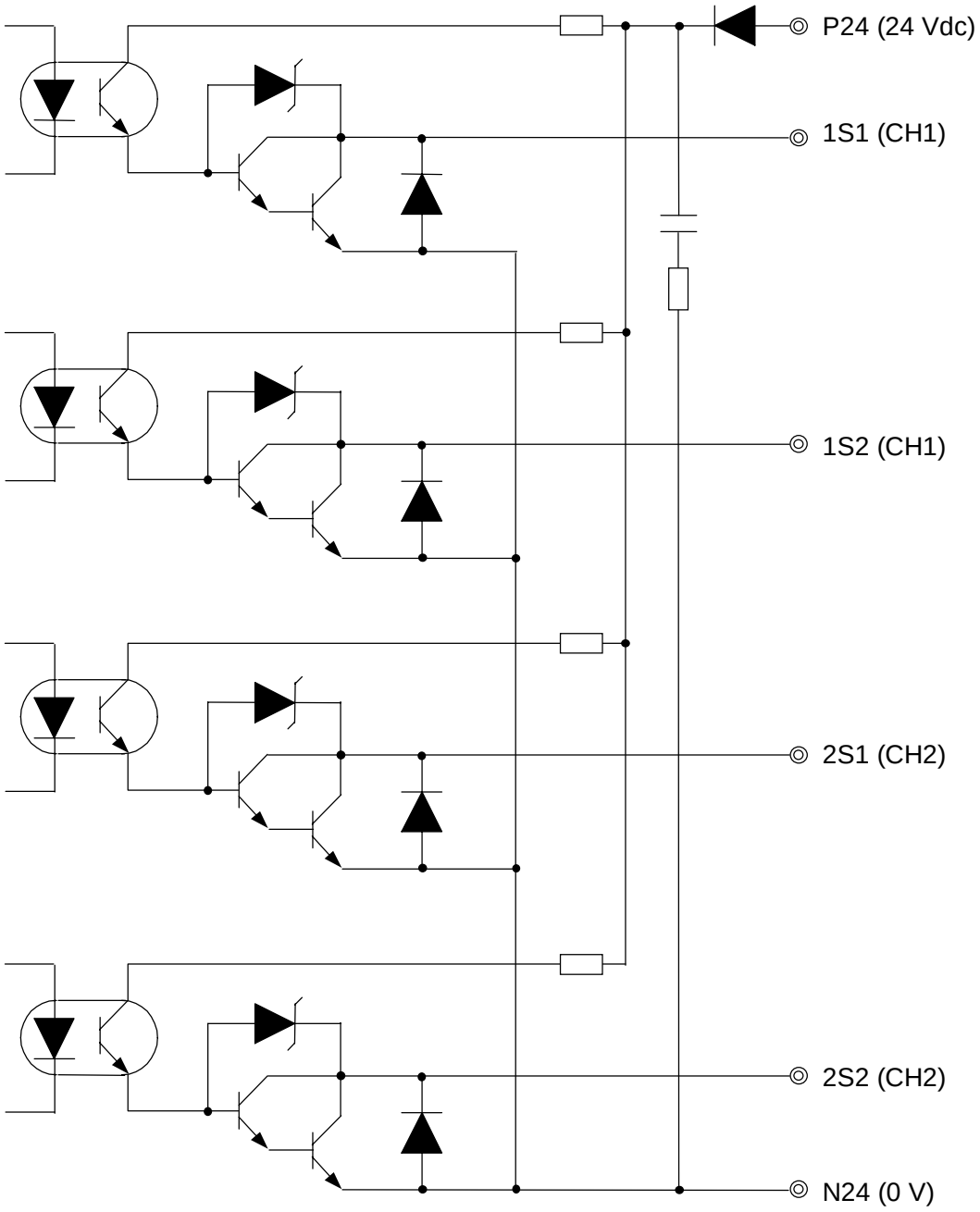


- **External limit input (EXT) < PI232/PI272 >**



- **Hardware comparison output circuit (1S1, 1S2, 2S1 and 2S2)**

  < PI232/PI272 >



Section 3

Wiring

3. Wiring

3.1 Connector pin assignment

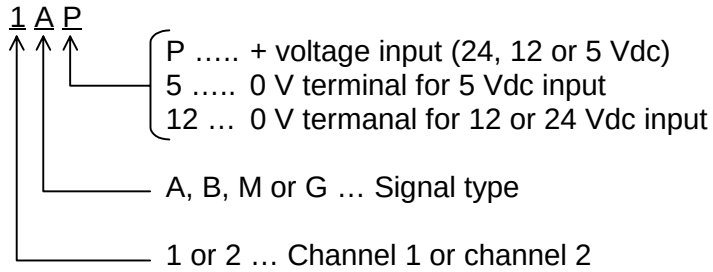
The following figure shows the pin assignment of the PI232/272's external signal connector.

< PI232 >

Function	Name	Pin No. A	Pin No. B	Name	Function
Channel 1 Phase A input	1A5	1	1	1AP	Channel 1 Phase A input
Channel 1 Phase B input	1BP	2	2	1A12	
	1B12	3	3	1B5	Channel 1 Phase B input
Channel 1 Maker input	1MP	4	4	1M5	Channel 1 Maker input
	1M12	5	5	2AP	Channel 2 Phase A input
Channel 2 Phase A input	2A5	6	6	2A12	
Channel 2 Phase B input	2BP	7	7	2B5	Channel 2 Phase B input
	2B12	8	8	2MP	Channel 2 Maker input
Channel 2 Maker input	2M5	9	9	2M12	
Channel 1 Gate input	1GP	10	10	1G5	Channel 1 Gate input
	1G12	11	11	2GP	Channel 2 Gate input
Channel 2 Gate input	2G5	12	12	2G12	
Channel 1 External limit input	1EXT-	13	13	1EXT+	Channel 1 External limit input
Channel 2 External limit input	2EXT-	14	14	2EXT+	Channel 2 External limit input
Channel 1 Compare output 2	1S2	15	15	1S1	Channel 1 Compare output 1
Channel 2 Compare output 2	2S2	16	16	2S1	Channel 2 Compare output 1
No use		17	17		No use
24 Vdc	P24	18	18	P24	24 Vdc
0 V for compare outputs	N24	19	19	N24	0 V for compare outputs
No use		20	20		No use

Remarks:

For phase A, B, zero maker and gate input, the signal name means as follows.



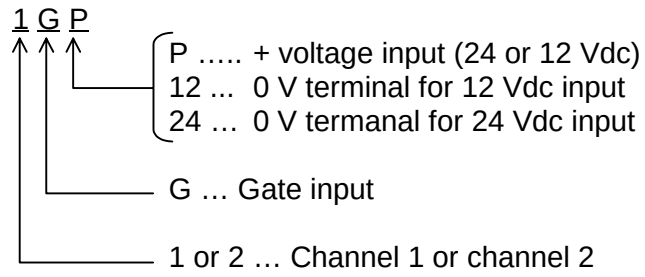
NOTE The cable side connector (soldering type) is standard accessory.

< PI272 >

Function	Name	Pin No. A	Pin No. B	Name	Function
Channel 1 Phase A +	1A+	1	1	1A–	Channel 1 Phase A –
Channel 1 Phase B +	1B+	2	2	1B–	Channel 1 Phase B –
Channel 1 Maker +	1M+	3	3	1M–	Channel 1 Maker –
Channel 2 Phase A +	2A+	4	4	2A–	Channel 2 Phase A –
Channel 2 Phase B +	2B+	5	5	2B–	Channel 2 Phase B –
Channel 2 Maker +	2M+	6	6	2M–	Channel 2 Maker –
Line receiver signal ground	SG	7	7	SG	Line receiver signal ground
Channel 1 Gate input	1G24	8	8	1G12	Channel 1 Gate input
	1GP	9	9	2GP	Channel 2 Gate input
Channel 2 Gate input	2G12	10	10	2G24	
No use		11	11		No use
Channel 1 Extermal limit input	1EXT-	12	12	1EXT+	Channel 1 External limit input
Channel 2 External limit input	2EXT-	13	13	2EXT+	Channel 2 External limit input
No use		14	14		No use
Channel 1 Compare output 2	1S2	15	15	1S1	Channel 1 Compare output 1
Channel 2 Compare output 2	2S2	16	16	2S1	Channel 2 Compare output 1
No use		17	17		No use
24 Vdc	P24	18	18	P24	24 Vdc
0 V for compare outputs	N24	19	19	N24	0 V for compare outputs
No use		20	20		No use

Remarks:

For gate input, the signal name means as follows.



NOTE The cable side connector (soldering type) is standard accessory.

3.2 Signal connections

Depending on the operation mode, required signals are different. This section shows how to connect each signal. Refer to your intended operation mode for which signal is used.

- **Pulse input signals**

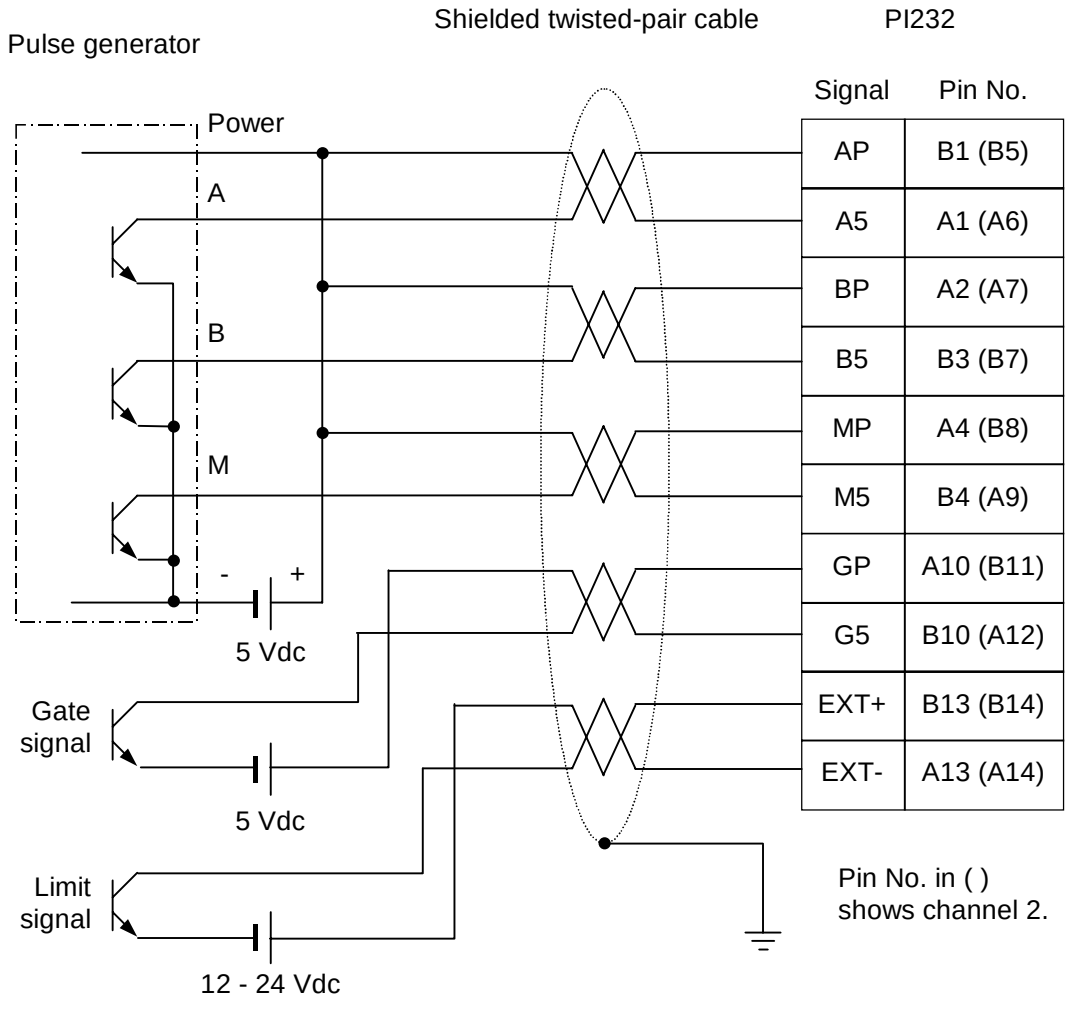
< PI232 >

Either 5 Vdc, 12 Vdc or 24 Vdc can be used for the signal voltage.
For 5 Vdc input, the terminals □P and □5 are used. (□ represents A, B, M or G)
For 12 Vdc or 24 Vdc, the terminals □P and □12 are used.
12 Vdc or 24 Vdc is selected by DIP switches W1 to W8. Refer to section 1.3.

When the voltage is applied between □P and □5 or between □P and □12, the PI232 recognizes the signal is ON.

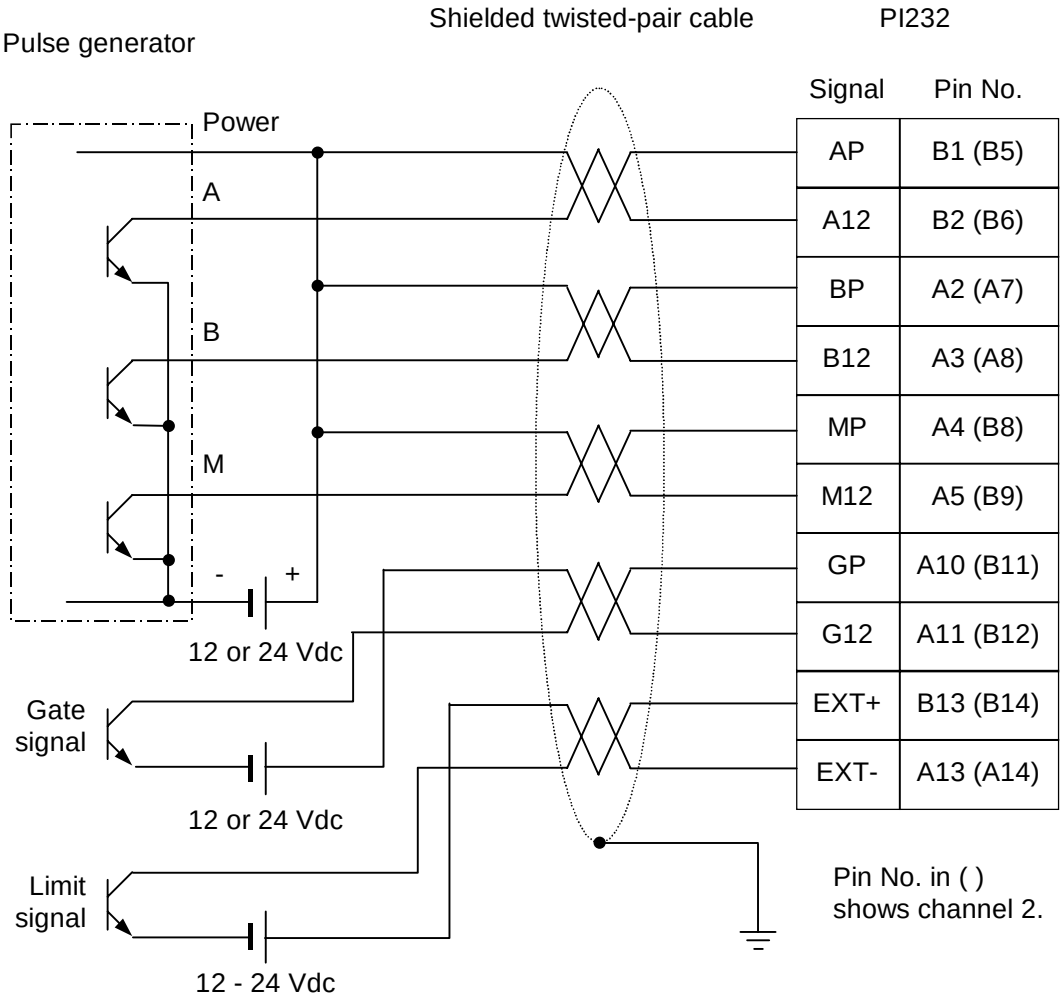
The figure below shows the typical connections for a channel.

In case of 5 Vdc input system:



< PI232 >

In case of 12 Vdc or 24 Vdc input system:



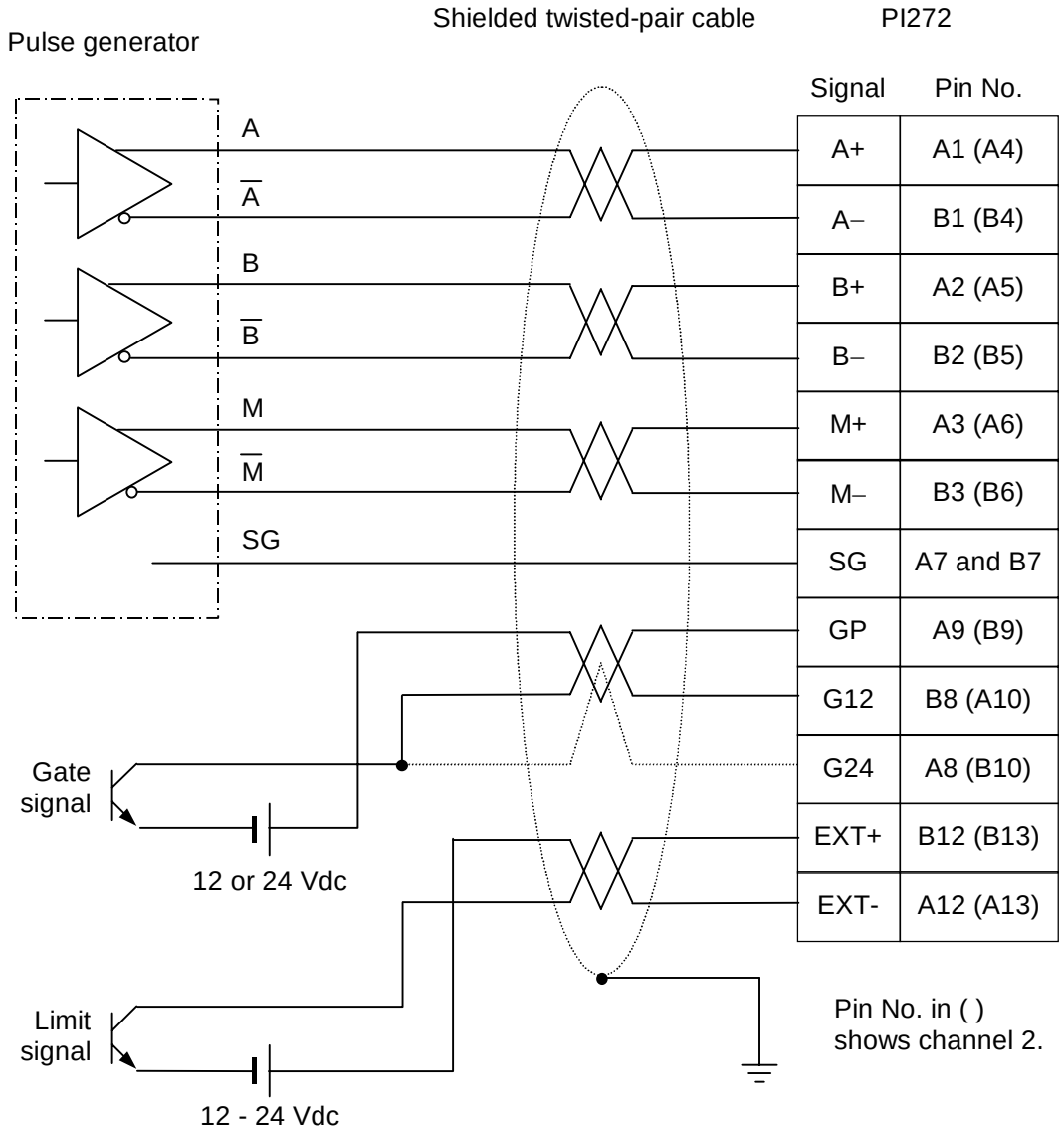
NOTE The input voltage for A, B, M, and G can be selected either 12 Vdc or 24 Vdc by setting the DIP switches provided on the PI232. Refer to section 1.3.

< PI272 >

Line driver type pulse generator is used with the PI272. The interface is RS-422-A. For the gate (G) input, either 12 Vdc or 24 Vdc can be used. For 12 Vdc, terminals GP and G12 are used. On the other hand, for 24 Vdc input, terminals GP and G24 are used.

When the voltage for □+ terminal is higher than □– terminal, the PI272 recognizes the signal is ON. (□ represents A, B or M)

The figure below shows the typical connections for a channel.



For the gate signal, either G12 or G24 terminal is used depending on the signal voltage. When it is 12 Vdc, use G12 terminal. And when it is 24 Vdc, use G24 terminal.

- **Hardware comparison output signals**

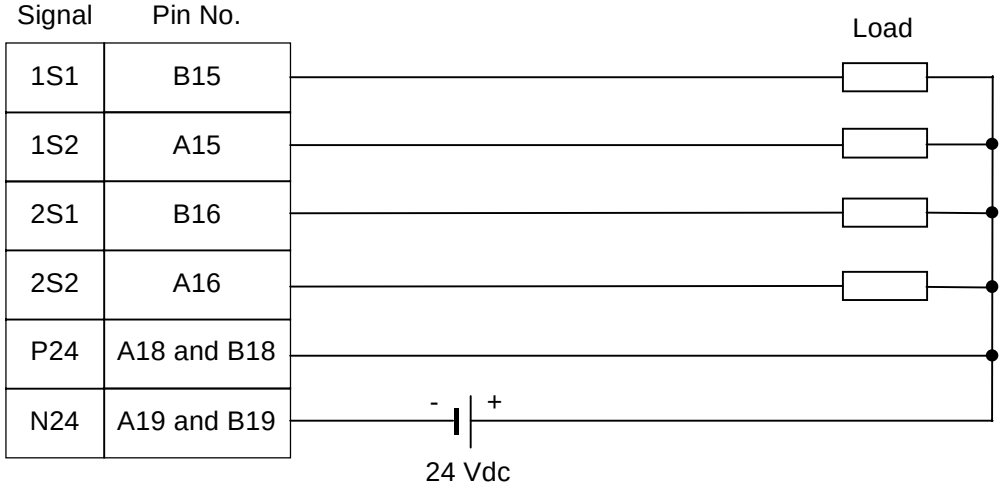
  2 points of hardware comparison output are provided for each channel. 1S1 and 1S2 are for channel 1, and 2S1 and 2S2 are for channel 2.

  The output method is 24 Vdc transistor output (current sinking).

  The figure below shows the typical wiring connections.

PI232/PI272

Signal	Pin No.
1S1	B15
1S2	A15
2S1	B16
2S2	A16
P24	A18 and B18
N24	A19 and B19



NOTE

(1) The hardware comparison output function is enabled when the output-enable flag is set to ON. Refer to section 4.1 for the output-enable flag.
(2) The 24 Vdc power is not required if the hardware comparison outputs are not used.

3.3 Wiring precautions

> ⚠ CAUTION
>
> Turn off power to the T2 and to the PI232/272 before wiring. Failure to do so can cause electrical shock or damage to the PI232/272.

- Use shielded twisted-pair cable for the pulse input signals to minimize interference of noise.
- Normally connect the cable shield to the T2's frame ground (unit mounting screw). However, in some cases, connection to the pulse generator's ground results more stable operation. In this case, disconnect the cable shield from the T2's frame ground and keep single-point grounding.
- The required signals are dependent on the PI232/272's operation mode. Check your operation mode for the necessary signals.

3. Wiring

Section 4

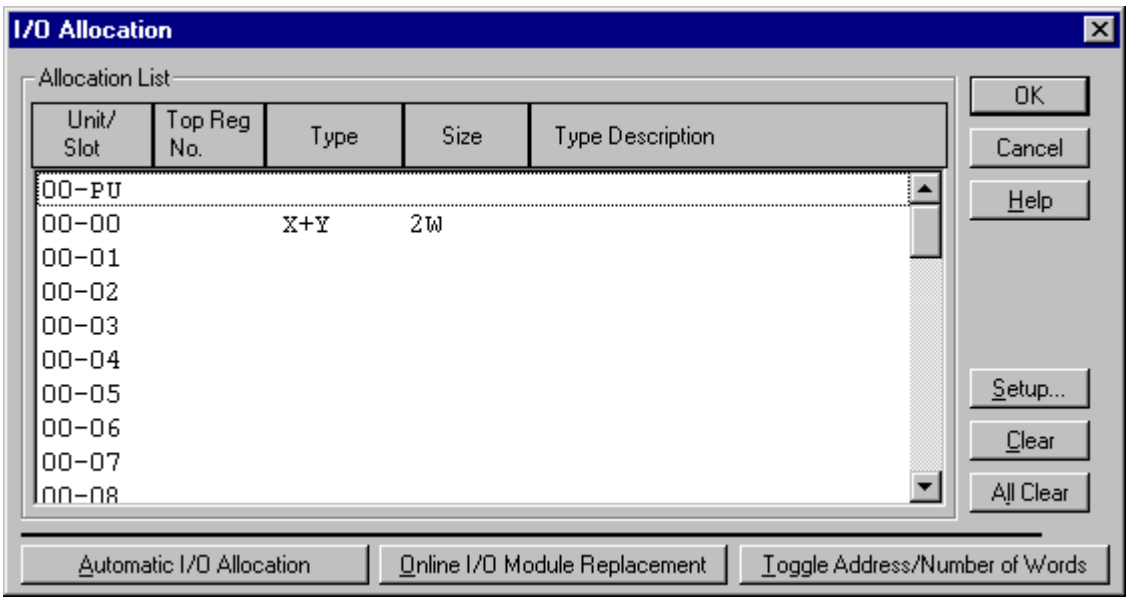
Register Configuration

4. Register Configuration

4.1 I/O allocation and I/O registers

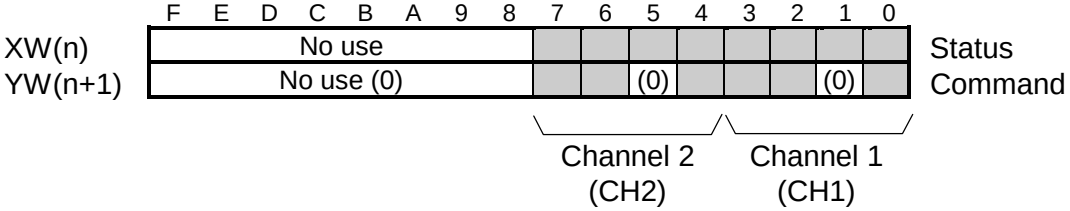
The PI232/272 has the I/O type '**X+Y 2W**' for I/O allocation. When the automatic I/O allocation is performed with mounting the PI232/272, the following I/O allocation table will be created in the T2.

(T-PDS screen example - in the case that PI232/272 is mounted on Slot 0 of Unit 0)



Then, 2 I/O registers, XW(n) and YW(n+1) are allocated to the PI232/272.
In the above example, XW000 and YW001 are allocated.

The following table shows the functions of I/O registers assigned to the PI232/272.



Register	Bit	Name	Description
XW(n)	F - 8	–	No use (data not defined)
	7	CH2 gate status	1: both gate input and soft-gate for CH 2 are ON
	6	CH2 EXT status	1: EXT input for CH2 is ON
	5	CH2 less than set-point-2	1: CH2 count value is less than the set-point-2
	4	CH2 greater than set-point- 1	1: CH2 count value is greater than the set-point-1
	3	CH1 gate status	1: both gate input and soft-gate for CH1 are ON
	2	CH1 EXT status	1: EXT input for CH1 is ON
	1	CH1 less than set-point-2	1: CH1 count value is less than the set-point-2
	0	CH1 greater than set-point- 1	1: CH1 count value is greater than the set-point-1
YW(n+1)	F - 8	–	No use (set to 0)
	7	CH2 input-disable	Set to 1 to disable CH2's count input
	6	CH2 output-enable	Set to 1 to enable CH2’s comparison outputs
	5	–	No use (set to 0)
	4	CH2 soft-gate	Set to 1 to enable CH2’s counter function
	3	CH1 input-disable	Set to 1 to disable CH1's count input
	2	CH1 output-enable	Set to 1 to enable CH1’s comparison outputs
	1	–	No use (set to 0)
	0	CH1 soft-gate	Set to 1 to enable CH1’s counter function

4. Register Configuration

4.2 PI232/272 buffer memory

The PI232/272's count value, set-point value, operation mode data, and other information are stored in the PI232/272's buffer memory.

This section explains the buffer memory contents and how to access the buffer memory.

4.2.1 Memory map

The PI232/272 has the buffer memory that is used to exchange data with T2. The memory map of the buffer memory is as follows.

Address	Word data	
H8000	Channel 1 count value	Channel 1 counter register (24-bit)
H8002	Channel 1 set-point-1	Channel 1 upper comparison value (24-bit)
H8004	Channel 1 set-point-2	Channel 1 lower comparison value (24-bit)
H8006	Channel 1 hold value	Channel 1 hold register (24-bit) (Read only)
H8008	Channel 2 count value	Channel 2 counter register (24-bit)
H800A	Channel 2 set-point-1	Channel 2 upper comparison value (24-bit)
H800C	Channel 2 set-point-2	Channel 2 lower comparison value (24-bit)
H800E	Channel 2 hold value	Channel 2 hold register (24-bit) (Read only)
H8010	Access inhibited	
H8018	Channel 1 mode	Channel 1 operation mode (16-bit) (Write only)
H8019	Channel 2 mode	Channel 2 operation mode (16-bit) (Write only)
H801A H803F	Access inhibited	

NOTE

The hold values (H8007·H8006 and H800F·H800E) are reading only.
On the other hand, the mode registers (H8018 and H8019) are writing only.
All other addresses are available for both reading and writing. (except the ranges of access inhibited)

4.2.2 Buffer memory access

T2 reads the PI232/272 buffer memory contents by using READ instruction (FUN237). And T2 writes data into the buffer memory by using WRITE instruction (FUN238).

READ instruction (FUN237)

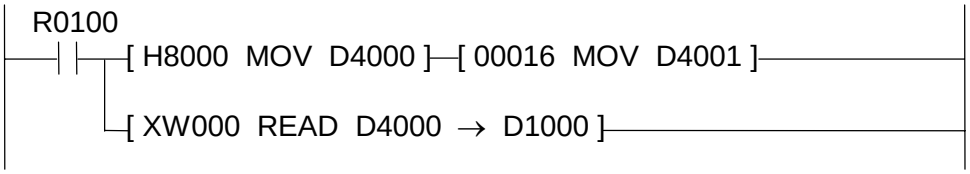
Expression:

—[(A) READ (B) → (C)]—

Operands:

(A): I/O register (XW/YW) assigned to the PI232/272
(B): Starting address of the buffer memory to be read
(B)+1: Number of words to be read (max. 16 for PI232/272)
(C): Starting register of the destination

Example:



When R0100 is ON, 16 words of buffer memory data starting with address H8000 are read from the PI232/272 which is allocated to XW000. And the data are stored in D1000 and after.

WRITE instruction (FUN238)

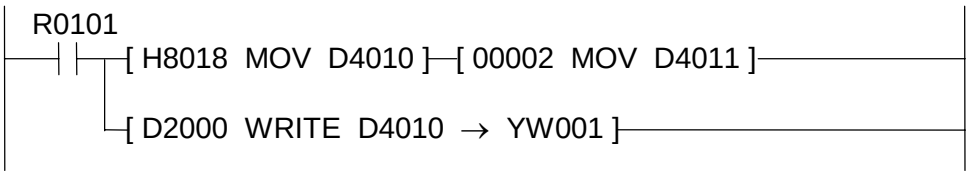
Expression:

—[(A) WRITE (B) → (C)]—

Operands:

(A): Starting register of the source
(B): Starting address of the buffer memory to be written
(B)+1: Number of words to be written (max. 6 for PI232/272)
(C): I/O register (XW/YW) assigned to the PI232/272

Example:

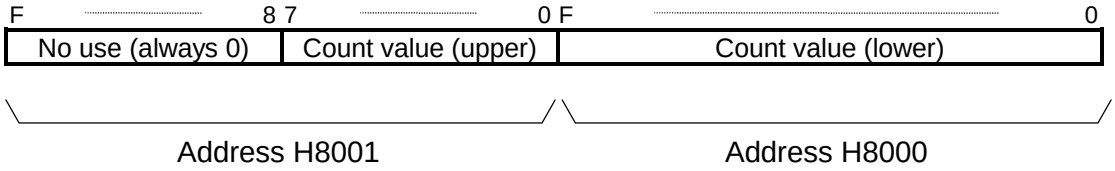


When R0101 is ON, 2 words of data starting with D2000 (D2000 and D2001) are written into the buffer memory address H8018 and H8019 of the PI232/272 which is allocated to YW001.

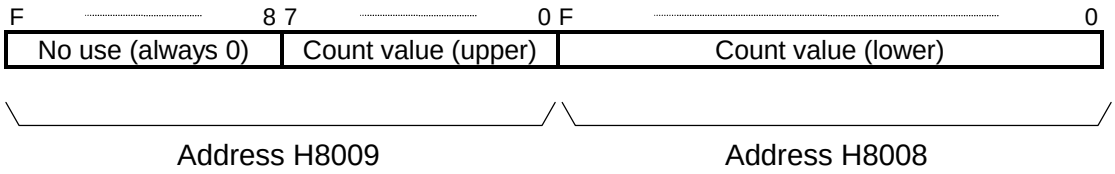
4.2.3 Count value registers

The addresses H8000, H8001 and H8008, H8009 store the count values for channel 1 and channel 2 respectively.
These data can be read into the T2 by READ instruction. Also, the T2 can write (change) the count values by WRITE instruction.

<Channel 1>



<Channel 2>



The count value is 24-bit length.
The lower address (address H8000 or H8008) stores the lower 16-bit of the count value.
The higher address (address H8001 or H8009) stores the upper 8-bit of the count value.
These subsequent 2 addresses configure 24-bit count value register. (the count value is 0 to 16777215)
The upper 8 bits of the higher address are all 0. When writing a double-word (32-bit) data into these addresses (presetting the count value), the upper 8 bits should be 0.

The count value registers are cleared to 0 at the timing of the gate condition is fulfilled.

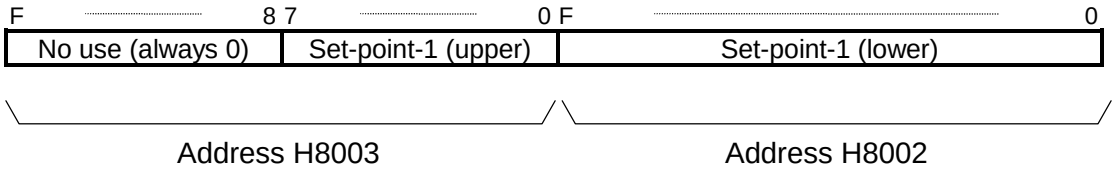
NOTE

In this manual, double-word (32-bit) register is expressed as,
{upper register} · {lower register}
For example;
D0011·D0010 ... for T2's register
H8009·H8008 ... for PI232/272's buffer memory address

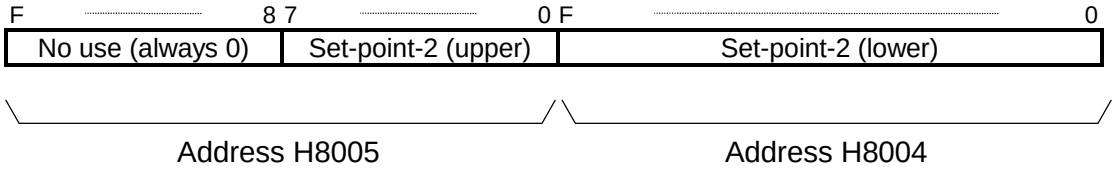
4.2.4 Upper and lower comparison value registers

The addresses H8002 through H8005 and H800A through H800D store the comparison values for channel 1 and channel 2 respectively.
The upper comparison value is called set-point-1, and the lower comparison value is called set-point-2. The function of these data is dependent on the counter operation mode.
These data can be written from the T2 by WRITE instruction. Also, the T2 can read these data by READ instruction.

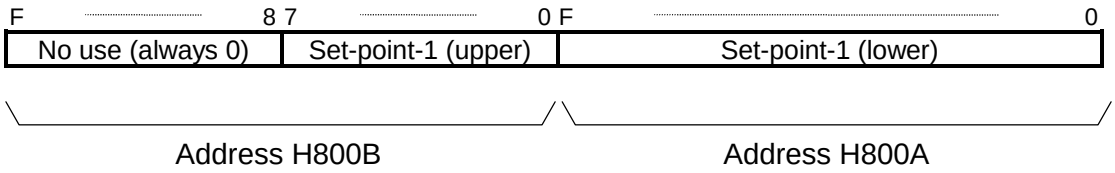
<Channel 1 - set-point-1>



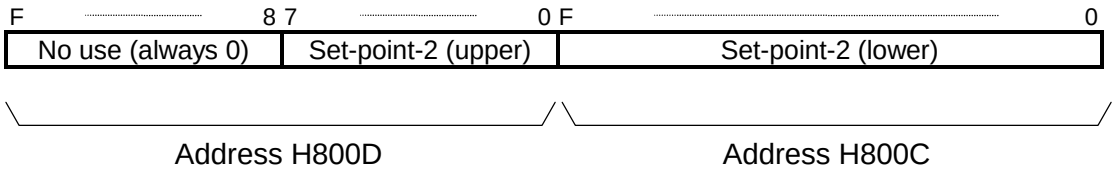
<Channel 1 - set-point-2>



<Channel 2 - set-point-1>



<Channel 2 - set-point-2>



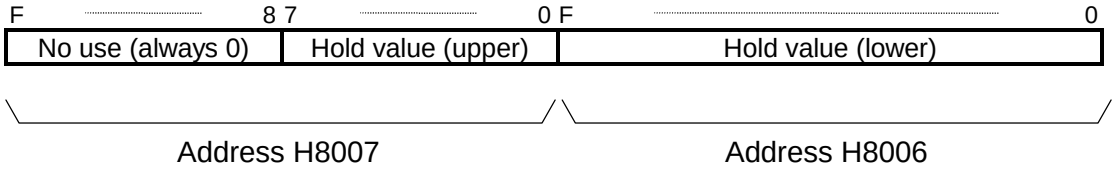
The comparison value (set-point-1 or -2) is 24-bit length.
The lower address stores the lower 16-bit of the comparison value. The higher address stores the upper 8-bit of the comparison value.
These subsequent 2 addresses configure 24-bit comparison value register.
The upper 8 bits of the higher address are all 0. When writing a double-word (32-bit) data into these addresses, the upper 8 bits should be 0.

The comparison value is internally set at the timing of the gate condition is fulfilled.

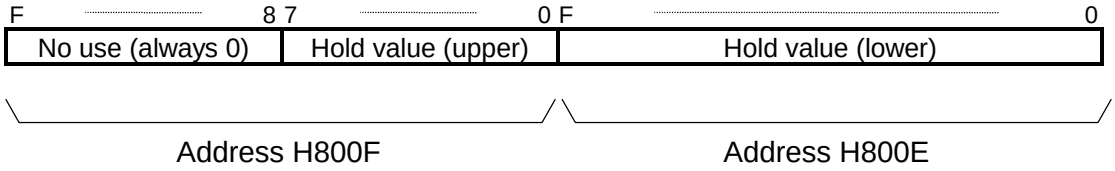
4.2.5 Hold value registers

The addresses H8006, H8007 and H800E, H800F store the hold values for channel 1 and channel 2 respectively.
These data can be read into the T2. Writing data into these addresses is prohibited.

<Channel 1>



<Channel 2>



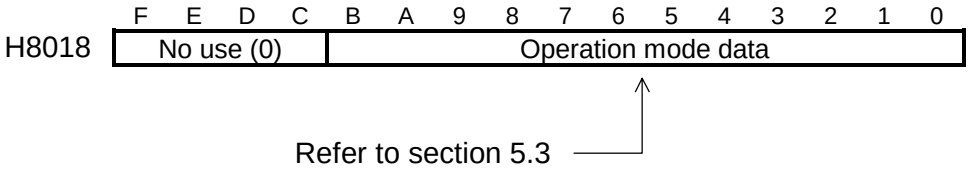
The hold value is 24-bit length.
The lower address stores the lower 16-bit of the hold value. The higher address stores the upper 8-bit of the hold value.
These subsequent 2 addresses configure 24-bit hold value register.
The upper 8 bits of the higher address are all 0.

The hold value registers are cleared to 0 at the timing of the gate condition is fulfilled.

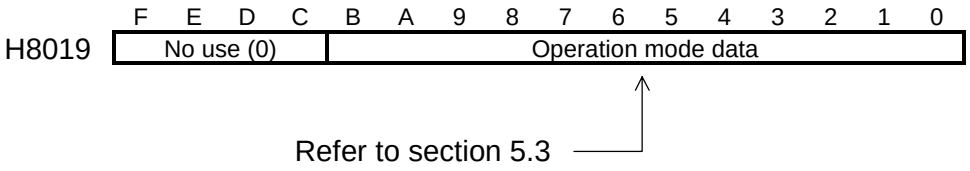
4.2.6 Operation mode registers

The channel 1 operation mode can be set by writing an appropriate data into the address H8018. And the channel 2 operation mode can be set by writing an appropriate data into the address H8019.
Operation mode setting is important to use the PI232/272. See section 5 for how to set the operation mode.
Reading data from these addresses is prohibited.

<Channel 1>



<Channel 2>



The operation mode is internally set at the timing of the gate condition is fulfilled.

Section 5

Operation Mode Setting

5. Operation Mode Setting

5.1 Mode setting overview

The PI232/272 has the following operation modes. The following a, b, c and d functions are selected in combination.

a. Counter operation mode

(1) Quadrature bi-pulse counter mode
(2) Up/down pulse counter mode
(3) Auto-reset universal counter mode
(4) Universal counter mode
(5) Speed counter mode (sampling time: 0.01s, 0.1s or 1s)
(6) Programmable interval timer mode (internal clock: 1 kHz, 10 kHz or 100 kHz)
(7) Gate-ON timer mode (internal clock: 1 kHz, 10 kHz or 100 kHz)

b. Pulse count mode

For the above each counter operation mode, the pulse count mode can be selected either normal count mode or precision count mode. Refer to section 1.2.2 for the pulse count mode.

c. Gate force

For the above counter operation mode except (7), the gate force function can be used. When the gate force is specified, the external Gate signal is recognized as always ON without need of actual Gate signal wiring.

d. Phase A/B exchange

For the above counter operation modes (1) and (2), function of phase A and phase B can be exchanged. That is, counting direction (up or down) can be changed by this setting.

To set the operation mode, the operation mode register in the PI232/272's buffer memory is used. There are 2 operation mode registers in the buffer memory. One is for channel 1 and the other is for channel 2.
Therefore, the operation mode can be set individually for channel 1 and channel 2. For example, you can set channel 1 to the quadrature bi-pulse counter and channel 2 to the speed counter.

5.2 Operation mode register setting

To use the PI232/272, it is important to set (write) a correct data into the operation mode register which is allocated on the PI232/272's buffer memory. (Refer to section 4.2.6)

Operation mode register:

<Channel 1>

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
H8018	No use (0)				Operation mode data											

<Channel 2>

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
H8019	No use (0)				Operation mode data											

The following tables show the operation mode data to be written into the operation mode register for setting each mode.

To write the data into the operation mode register, WRITE instruction (FUN238) is used.

Operation mode data:

In the following tables, the number in brackets ( ) on the operation mode data column shows the decimal value of the operation mode data.

(1) Quadrature bi-pulse counter mode

Phase A/B exchange	Gate force	Pulse count mode	Operation mode data
Normal	Normal	Normal	H0002 (2)
		Precision	H0042 (66)
	Forced	Normal	H0102 (258)
		Precision	H0142 (322)
Exchange	Normal	Normal	H0802 (2050)
		Precision	H0842 (2114)
	Forced	Normal	H0902 (2306)
		Precision	H0942 (2370)

(2) Up/down pulse counter mode

Phase A/B exchange	Gate force	Pulse count mode	Operation mode data
Normal	Normal	Normal	H0000 (0)
		Precision	H0040 (64)
	Forced	Normal	H0100 (256)
		Precision	H0140 (320)
Exchange	Normal	Normal	H0800 (2048)
		Precision	H0840 (2112)
	Forced	Normal	H0900 (2304)
		Precision	H0940 (2368)

(3) Auto-reset universal counter mode

Gate force	Pulse count mode	Operation mode data
Normal	Normal	H0081 (129)
	Precision	H00C1 (193)
Forced	Normal	H0181 (385)
	Precision	H01C1 (449)

(4) Universal counter mode

Gate force	Pulse count mode	Operation mode data
Normal	Normal	H0001 (1)
	Precision	H0041 (65)
Forced	Normal	H0101 (257)
	Precision	H0141 (321)

(5) Speed counter mode

Pulse count mode	Sampling time	Operation mode data
Normal	0.01 s	H0005 (5)
	0.1 s	H0205 (517)
	1 s	H0405 (1029)
Precision	0.01 s	H0045 (69)
	0.1 s	H0245 (581)
	1 s	H0445 (1093)

(6) Programmable interval timer mode

Gate force	Pulse count mode	Internal clock	Operation mode data
Normal	Normal	1 kHz	H0091 (145)
		10 kHz	H00A1 (161)
		100 kHz	H00B1 (177)
	Precision	1 kHz	H00D1 (209)
		10 kHz	H00E1 (225)
		100 kHz	H00F1 (241)
Forced	Normal	1 kHz	H0191 (401)
		10 kHz	H01A1 (417)
		100 kHz	H01B1 (433)
	Precision	1 kHz	H01D1 (465)
		10 kHz	H01E1 (481)
		100 kHz	H01F1 (497)

(7) Gate-ON timer mode

Pulse count mode	Internal clock	Operation mode data
Normal	1 kHz	H0011 (17)
	10 kHz	H0021 (33)
	100 kHz	H0031 (49)
Precision	1 kHz	H0051 (81)
	10 kHz	H0061 (97)
	100 kHz	H0071 (113)

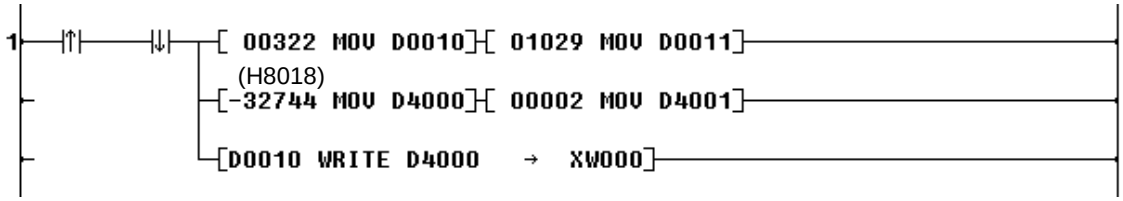
5. Operation Mode Setting

T2 sample programs to set the operation modes are shown below.
In these sample programs, the PI232/272's operation modes are set at the second scan of the T2 program execution.

Sample 1:

This program sets channel 1 to the quadrature bi-pulse counter of precision pulse count mode with gate forced (phase A/B exchange is normal) , and channel 2 to the 1 second speed counter of normal pulse count mode.

It is assumed that the PI232/272 is allocated to XW000 and YW001.

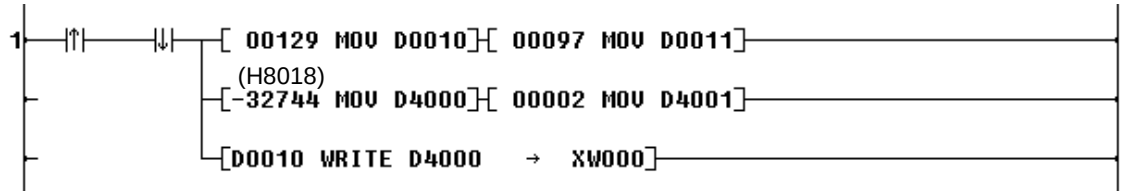


By executing this program, the data 322 (H0142) and 1029 (H0405) are written into the addresses H8018 and H8019 of the PI232/272's buffer memory respectively at the second scan.

Sample 2:

This program sets channel 1 to the auto-reset universal counter of normal pulse count mode without gate force function, and channel 2 to the gate ON timer with using 10 kHz clock of precision pulse count mode.

It is assumed that the PI232/272 is allocated to XW000 and YW001.



By executing this program, the data 129 (H0081) and 97 (H0061) are written into the addresses H8018 and H8019 of the PI232/272's buffer memory respectively at the second scan.

NOTE

Any writing operation into the PI232/272's buffer memory is prohibited during the first scan. Therefore the mode setting circuit must be executed at the second scan or later.

Section 6

Function Details

6. Function Details

6.1 Quadrature bi-pulse counter mode

(1) Mode setting

Phase A/B exchange	Gate force	Pulse count mode	Operation mode data
Normal	Normal	Normal	H0002 (2)
		Precision	H0042 (66)
	Forced	Normal	H0102 (258)
		Precision	H0142 (322)
Exchange	Normal	Normal	H0802 (2050)
		Precision	H0842 (2114)
	Forced	Normal	H0902 (2306)
		Precision	H0942 (2370)

(2) External signals

Signal	Function
Phase A	Quadrature pulses Counting up when phase A precedes (at normal)
Phase B	Counting down when phase B precedes (at normal)
Marker	Can be used to clear the count value (cleared at the rising edge of Marker while EXT is ON)
Gate	Used to enable the counter operation (not necessary if gate force is used) (counter operation is enabled when both external gate and soft-gate are ON)
EXT	Can be used to clear the count value (see Marker)
S1	Hardware comparison output Comes ON when count value > set-point-1
S2	Hardware comparison output Comes ON when count value < set-point-2

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Can be used for hardware comparison output (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	
Hold value	H8007·H8006 / H800F·H800E	Stores the hold value (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled when both external gate and soft-gate are ON)
Output-enable	2 / 6	Set to ON to enable hardware comparison outputs
Input-disable	3 / 7	Set to ON to disable pulse count

(5) Operation

PI232/272 counts the pulses whose phases are shifted 90° each other.
In the normal condition, the PI232/272 counts up (increase) when phase A pulse precedes against phase B pulse, and the PI232/272 counts down (decrease) when phase B pulse precedes.

PI232/272 can count up to 50 kHz pulses. Therefore the maximum counting speed is as follows.

Normal count mode: 50 k counts per second
Precision count mode: 200 k counts per second

This mode function is enabled while both external gate and soft-gate are ON.
If the gate force function is used, this mode function is enabled by soft-gate ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

The count value can be changed by directly writing a data into the buffer memory.
Also, the count value is cleared to 0 by hardware at the following timing.

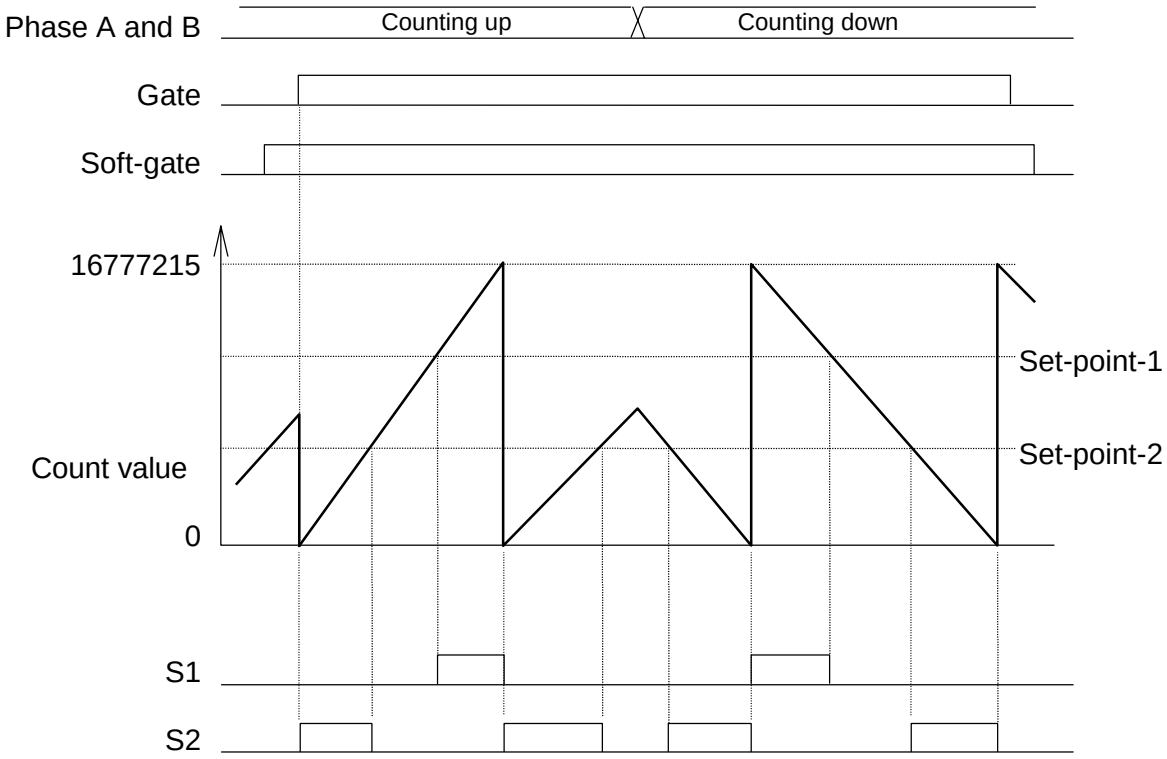
a) At the moment of gate condition is fulfilled
b) At the moment of Maker comes ON while EXT is ON
(EXT must be ON at least 100 ms before Maker comes ON)

When an up count comes at the count value is upper limit (16777215), the count value is reset to 0. When a down count comes at the count value is lower limit (0), the count value is reset to the upper limit value (16777215).

When the output-enable bit in the command register (YW) is ON, the hardware comparison outputs (S1 and S2) are enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON. And when the count value is smaller than the set-point-2, S2 comes ON.

When the input-disable bit in the command register (YW) is ON, PI232/272 stops the pulse counting.

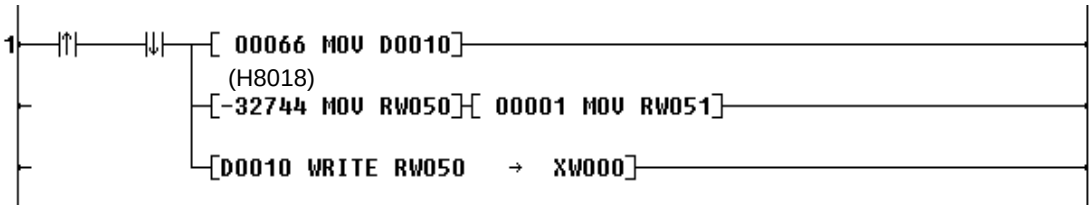
When the gate condition comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

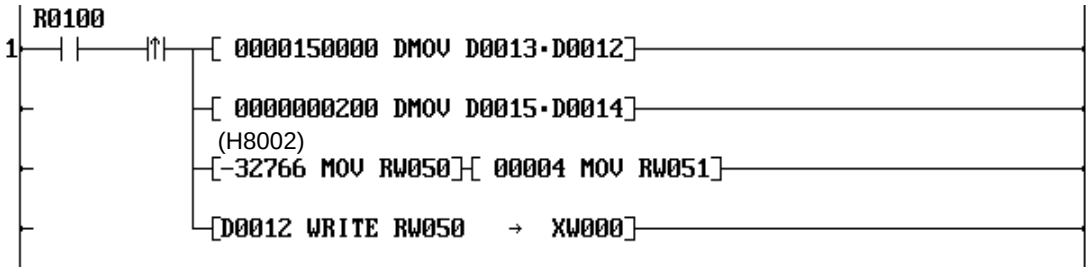
- Setting the quadrature bi-pulse counter mode for channel 1
  (pulse mode = precision, gate force = no, phase A/B = normal)



At the beginning of RUN mode (at the second scan), the mode data 66 (H0042) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

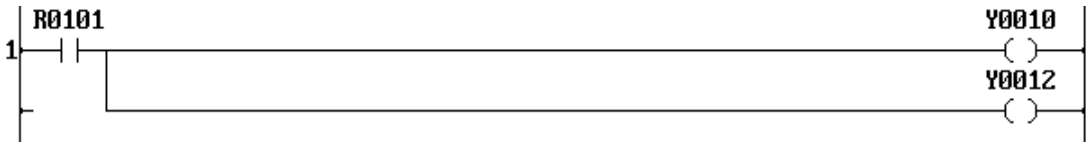
  Channel 1 Set-point-1 = 150000
  Set-point-2 = 200



  At the rising edge of R0100 coming ON, the data 150000 and 200 are written into the addresses H8003·H8002 (CH1 set-point-1) and H8005·H8004 (CH1 set-point-2).

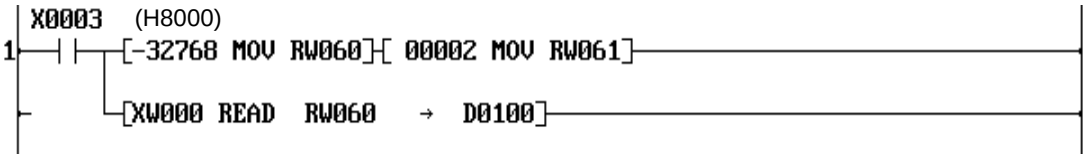
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON
  Output-enable (Y0012) = ON



  When R0101 is ON, Y0010 and Y0012 are set to ON.

- Reading the count value



  When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101·D0100.

6.2 Up/down pulse counter mode

(1) Mode setting

Phase A/B exchange	Gate force	Pulse count mode	Operation mode data
Normal	Normal	Normal	H0000 (0)
		Precision	H0040 (64)
	Forced	Normal	H0100 (256)
		Precision	H0140 (320)
Exchange	Normal	Normal	H0800 (2048)
		Precision	H0840 (2112)
	Forced	Normal	H0900 (2304)
		Precision	H0940 (2368)

(2) External signals

Signal	Function
Phase A	Counting up pulse (at normal)
Phase B	Counting down pulse (at normal)
Marker	Can be used to clear the count value (cleared at the rising edge of Marker while EXT is ON)
Gate	Used to enable the counter operation (not necessary if gate force is used) (counter operation is enabled when both external gate and soft-gate are ON)
EXT	Can be used to clear the count value (see Marker)
S1	Hardware comparison output Comes ON when count value > set-point-1
S2	Hardware comparison output Comes ON when count value < set-point-2

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Can be used for hardware comparison output (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	
Hold value	H8007·H8006 / H800F·H800E	Stores the hold value (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled when both external gate and soft-gate are ON)
Output-enable	2 / 6	Set to ON to enable hardware comparison outputs
Input-disable	3 / 7	Set to ON to disable pulse count

(5) Operation

PI232/272 counts the pulses phase A and phase B.
In the normal condition, phase A is counting up (increase), and phase B is counting down (decrease). When both phase A and phase B come ON simultaneously, counting is not executed.

In the normal count mode, PI232/272 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.
PI232/272 can count up to 100 kHz pulses. Therefore the maximum counting speed is as follows.

Normal count mode: 100 k counts per second
Precision count mode: 200 k counts per second

This mode function is enabled while both external gate and soft-gate are ON.
If the gate force function is used, this mode function is enabled by soft-gate ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

The count value can be changed by directly writing a data into the buffer memory. Also, the count value is cleared to 0 by hardware at the following timing.

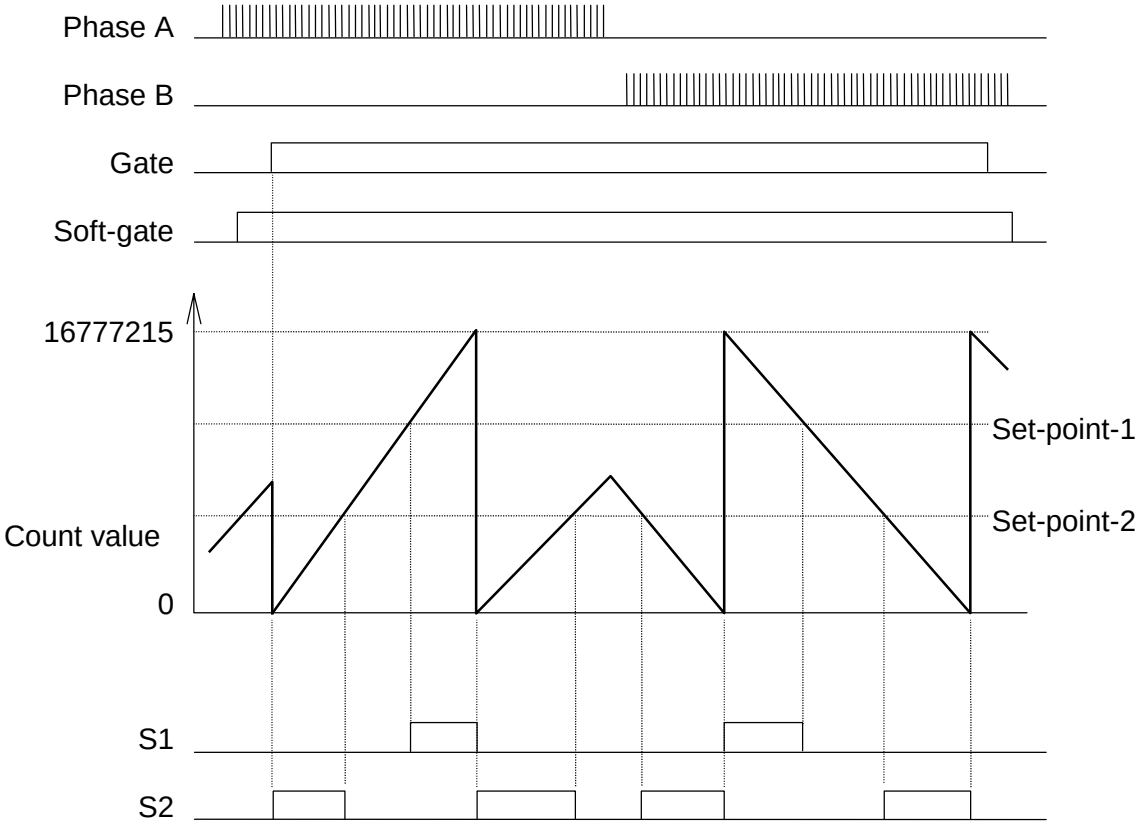
a) At the moment of gate condition is fulfilled
b) At the moment of Marker comes ON while EXT is ON
(EXT must be ON at least 100 ms before Marker comes ON)

When an up count comes at the count value is upper limit (16777215), the count value is reset to 0. When a down count comes at the count value is lower limit (0), the count value is reset to the upper limit value (16777215).

When the output-enable bit in the command register (YW) is ON, the hardware comparison outputs (S1 and S2) are enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON. And when the count value is smaller than the set-point-2, S2 comes ON.

When the input-disable bit in the command register (YW) is ON, PI232/272 stops the pulse counting.

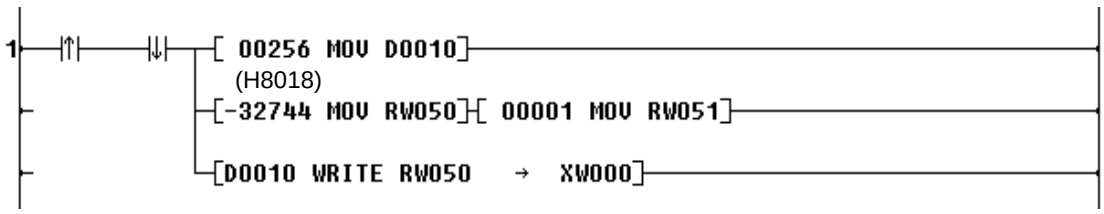
When the gate condition comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

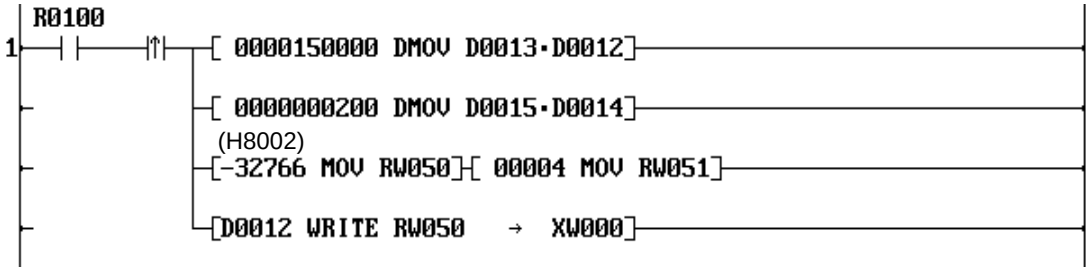
- Setting the up/down pulse counter mode for channel 1
  (pulse mode = normal, gate force = forced, phase A/B = normal)



At the beginning of RUN mode (at the second scan), the mode data 256 (H0100) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

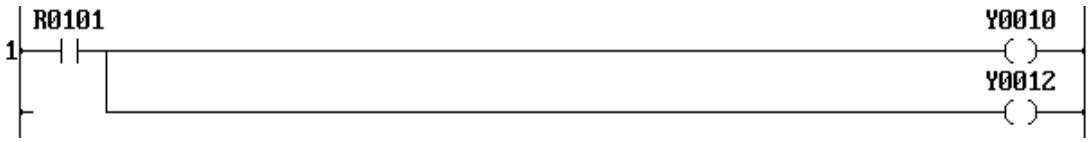
  Channel 1 Set-point-1 = 150000
  Set-point-2 = 200



At the rising edge of R0100 coming ON, the data 150000 and 200 are written into the addresses H8003·H8002 (CH1 set-point-1) and H8005·H8004 (CH1 set-point-2).

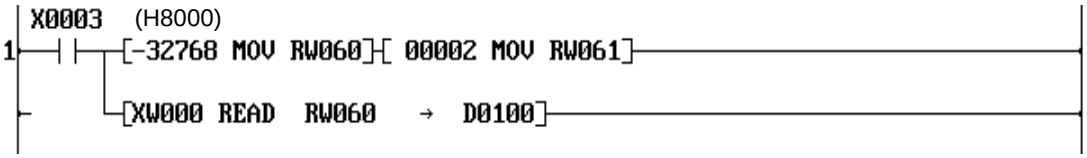
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON
  Output-enable (Y0012) = ON



When R0101 is ON, Y0010 and Y0012 are set to ON.

- Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101·D0100.

6.3 Auto-reset universal counter mode

(1) Mode setting

Gate force	Pulse count mode	Operation mode data
Normal	Normal	H0081 (129)
	Precision	H00C1 (193)
Forced	Normal	H0181 (385)
	Precision	H01C1 (449)

(2) External signals

Signal	Function
Phase A	Counting up pulse
Phase B	No use
Marker	No use
Gate	Used to enable the counter operation (not necessary if gate force is used) (counter operation is enabled when both external gate and soft-gate are ON)
EXT	No use
S1	No use
S2	No use

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Used to set the reset point (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	No use
Hold value	H8007·H8006 / H800F·H800E	Stores the hold value (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled when both external gate and soft-gate are ON)
Output-enable	2 / 6	No use
Input-disable	3 / 7	Set to ON to disable pulse count

(5) Operation

PI232/272 counts up by the single phase pulses into phase A.

In the normal count mode, PI232/272 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.
PI232/272 can count up to 100 kHz pulses. Therefore the maximum counting speed is as follows.

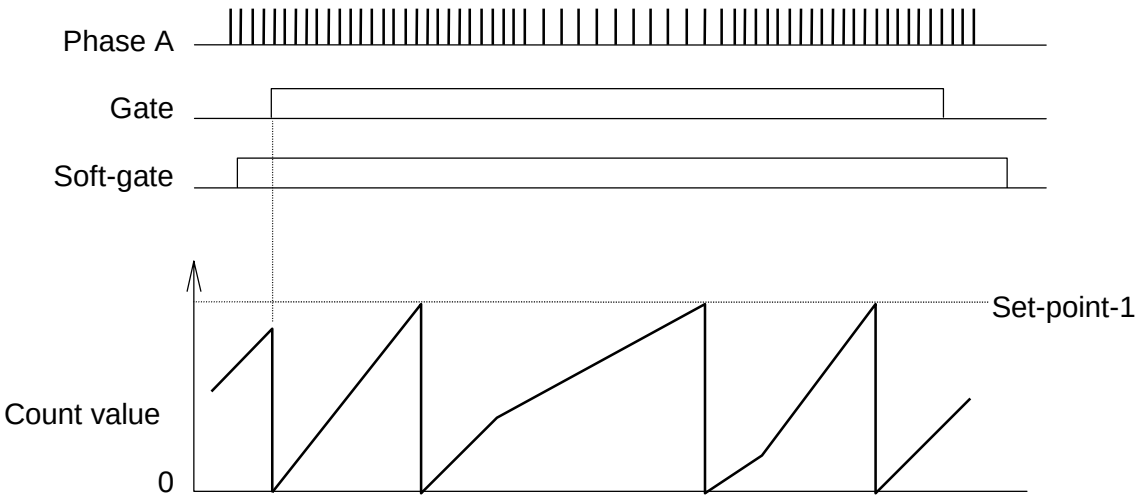
Normal count mode: 100 k counts per second
Precision count mode: 200 k counts per second

This mode function is enabled while both external gate and soft-gate are ON.
If the gate force function is used, this mode function is enabled by soft-gate ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

The count value is cleared to 0 at the timing of gate condition is fulfilled.
Also, the count value can be changed by directly writing a data into the buffer memory.

When the count value reaches the set-point-1, the count value is reset to 0 (zero).
The set-point-1 can be set in the range of 1 to 16777215.

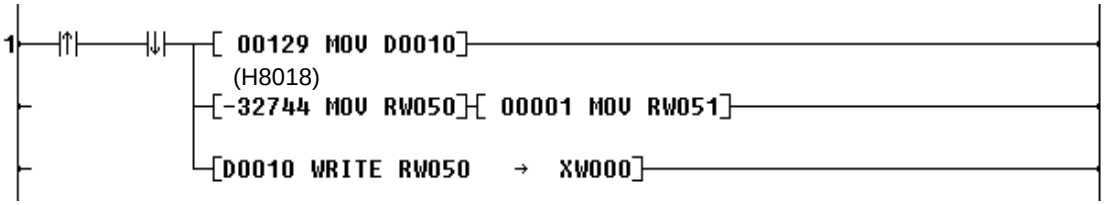
When the gate condition comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

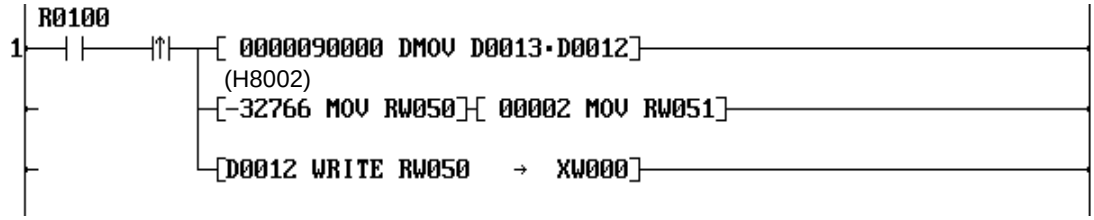
- Setting the auto-reset universal counter mode for channel 1
  (pulse mode = normal, gate force = no)



At the beginning of RUN mode (at the second scan), the mode data 129 (H0081) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

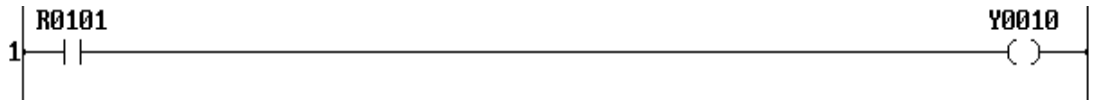
  Channel 1 Set-point-1 = 90000



At the rising edge of R0100 coming ON, the data 90000 is written into the addresses H8003·H8002 (CH1 set-point-1).

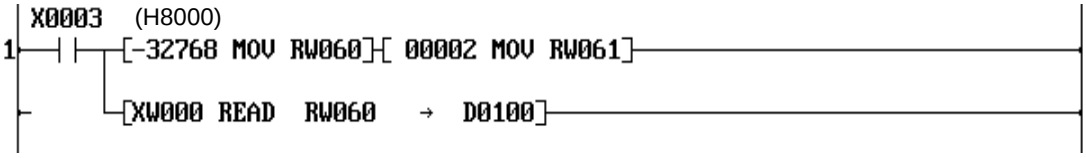
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON



When R0101 is ON, Y0010 is set to ON.

- Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101·D0100.
To use the status register (XW000), direct I/O instruction is necessary in the program.

6.4 Universal counter mode

(1) Mode setting

Gate force	Pulse count mode	Operation mode data
Normal	Normal	H0001 (1)
	Precision	H0041 (65)
Forced	Normal	H0101 (257)
	Precision	H0141 (321)

(2) External signals

Signal	Function
Phase A	Counting up pulse
Phase B	No use
Marker	No use
Gate	Used to enable the counter operation (not necessary if gate force is used) (counter operation is enabled when both external gate and soft-gate are ON)
EXT	No use
S1	Hardware comparison output Comes ON when count value > set-point-1
S2	No use

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Can be used for hardware comparison output (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	No use
Hold value	H8007·H8006 / H800F·H800E	Stores the hold value (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled when both external gate and soft-gate are ON)
Output-enable	2 / 6	Set to ON to enable hardware comparison output
Input-disable	3 / 7	Set to ON to disable pulse count

(5) Operation

PI232/272 counts up by the single phase pulses into phase A.

In the normal count mode, PI232/272 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.
PI232/272 can count up to 100 kHz pulses. Therefore the maximum counting speed is as follows.

Normal count mode: 100 k counts per second
Precision count mode: 200 k counts per second

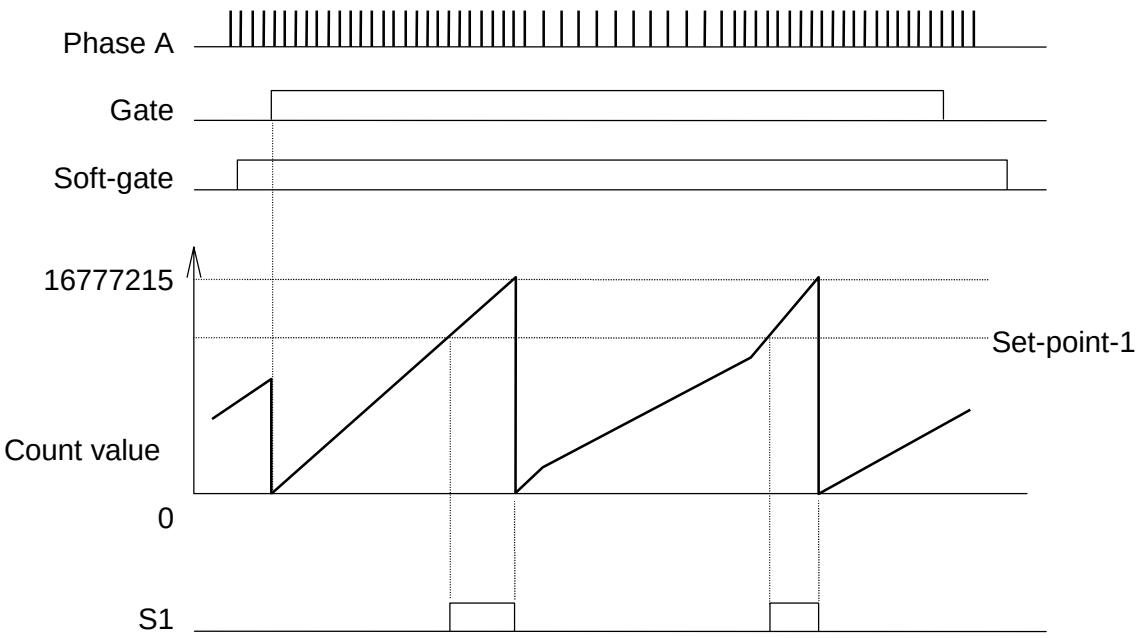
This mode function is enabled while both external gate and soft-gate are ON.
If the gate force function is used, this mode function is enabled by soft-gate ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

The count value is cleared to 0 at the timing of gate condition is fulfilled.
Also, the count value can be changed by directly writing a data into the buffer memory.

When the count value exceeds the upper limit value (16777215), it is reset to 0 (zero).

When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.

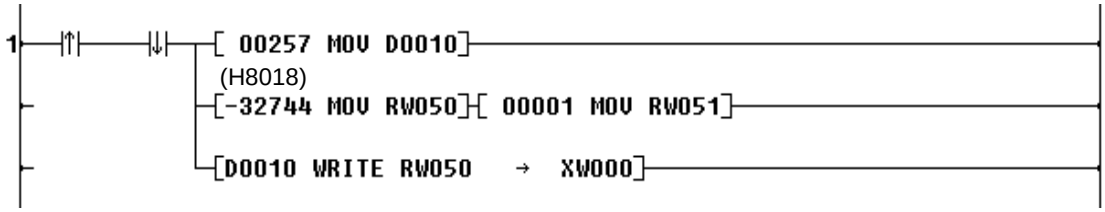
When the gate condition comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

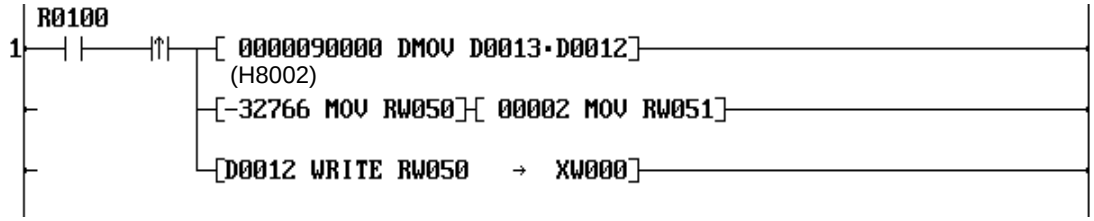
- Setting the universal counter mode for channel 1
  (pulse mode = normal, gate force = forced)



At the beginning of RUN mode (at the second scan), the mode data 257 (H0101) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

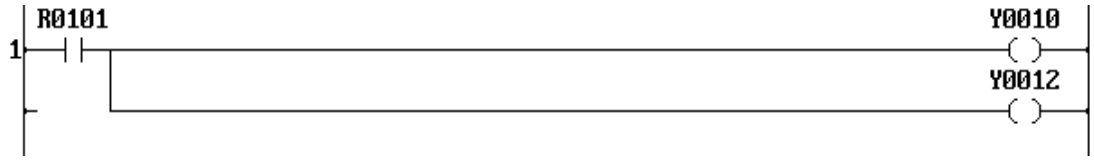
  Channel 1 Set-point-1 = 90000



At the rising edge of R0100 coming ON, the data 90000 is written into the addresses H8003·H8002 (CH1 set-point-1).

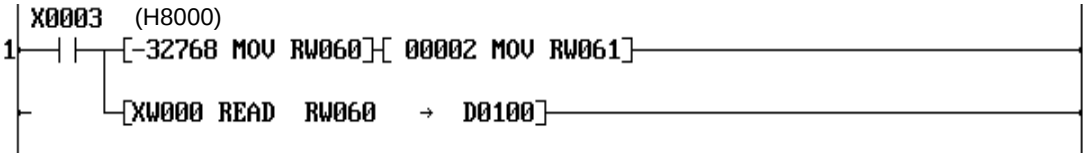
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON
  Output-enable (Y0012) = ON



When R0101 is ON, Y0010 and Y0012 are set to ON.

- Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101·D0100.
To use the status register (XW000), direct I/O instruction is necessary in the program.

6.5 Speed counter mode

(1) Mode setting

Pulse count mode	Sampling time	Operation mode data
Normal	0.01 s	H0005 (5)
	0.1 s	H0205 (517)
	1 s	H0405 (1029)
Precision	0.01 s	H0045 (69)
	0.1 s	H0245 (581)
	1 s	H0445 (1093)

(2) External signals

Signal	Function
Phase A	Counting up pulse
Phase B	No use
Marker	No use
Gate	No use
EXT	No use
S1	Hardware comparison output Comes ON when count value > set-point-1
S2	No use

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Can be used for hardware comparison output (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	No use
Hold value	H8007·H8006 / H800F·H800E	Stores the count value in a sampling time (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled while ON)
Output-enable	2 / 6	Set to ON to enable hardware comparison output
Input-disable	3 / 7	Set to ON to disable pulse count

(5) Operation

PI232/272 counts the single phase pulses into phase A during the specified sampling time.

The sampling time can be selected from 0.01, 0.1 or 1 second.

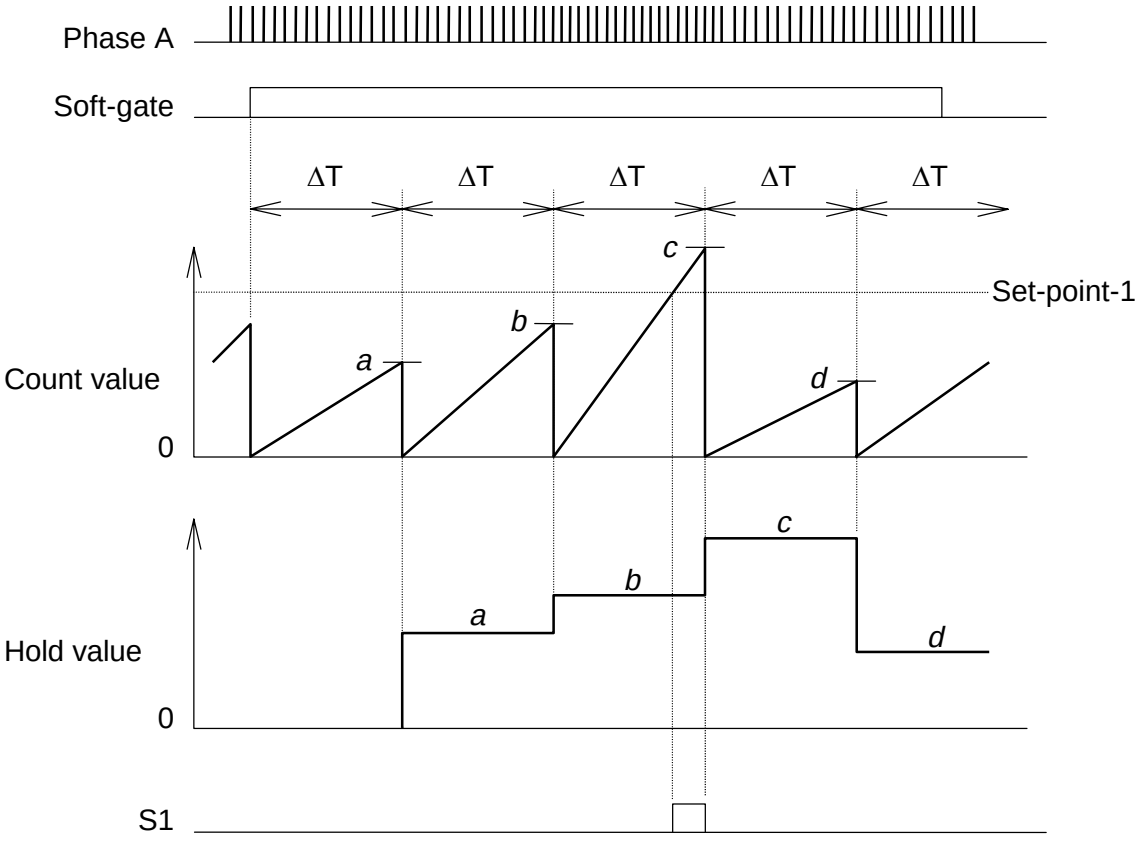
In the normal count mode, PI232/272 counts at the rising edge of the pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the pulse. Therefore the count value becomes double in the precision count mode.
PI232/272 can count up to 100 kHz pulses. Therefore the maximum counting speed is as follows.

Normal count mode: 100 k counts per second
Precision count mode: 200 k counts per second

This mode function is enabled while soft-gate is ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

The count value in a sampling time is transferred into the hold register. By reading the hold register, the pulse rate can be measured.

When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.

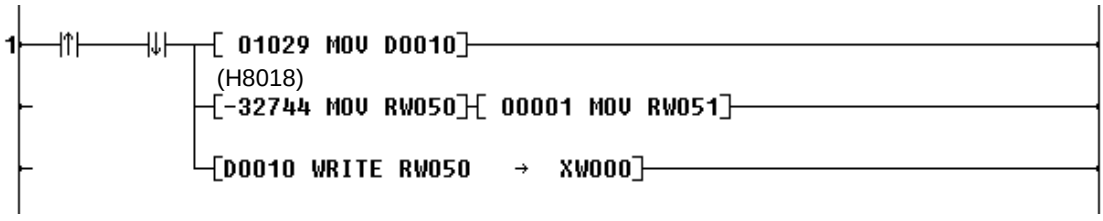


ΔT: sampling time = 0.01s, 0.1s or 1 s

(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

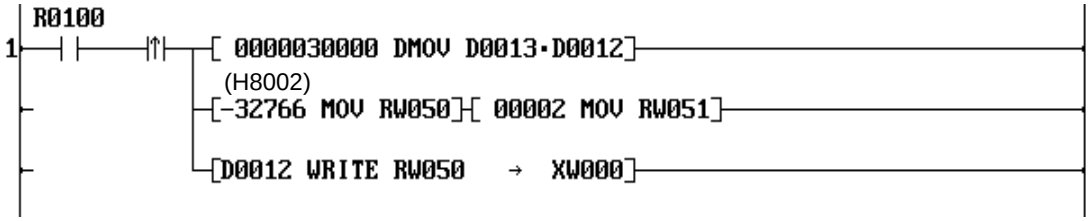
- Setting the 1 second sampling speed counter mode for channel 1 (pulse mode = normal)



At the beginning of RUN mode (at the second scan), the mode data 1029 (H0405) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

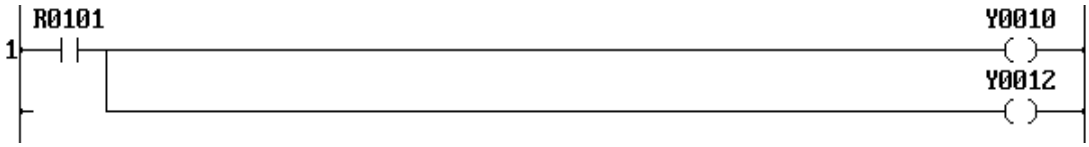
  Channel 1 Set-point-1 = 30000



  At the rising edge of R0100 coming ON, the data 30000 is written into the addresses H8003·H8002 (CH1 set-point-1).

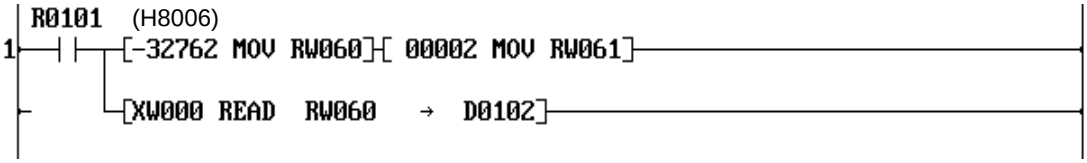
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON
  Output-enable (Y0012) = ON



  When R0101 is ON, Y0010 and Y0012 are set to ON.

- Reading the hold value



  When R0101 is ON, the hold value is read and stored in the double-word register D0103·D0102.

6.6 Programmable interval timer mode

(1) Mode setting

Gate force	Pulse count mode	Internal clock	Operation mode data
Normal	Normal	1 kHz	H0091 (145)
		10 kHz	H00A1 (161)
		100 kHz	H00B1 (177)
	Precision	1 kHz	H00D1 (209)
		10 kHz	H00E1 (225)
		100 kHz	H00F1 (241)
Forced	Normal	1 kHz	H0191 (401)
		10 kHz	H01A1 (417)
		100 kHz	H01B1 (433)
	Precision	1 kHz	H01D1 (465)
		10 kHz	H01E1 (481)
		100 kHz	H01F1 (497)

(2) External signals

Signal	Function
Phase A	No use
Phase B	No use
Marker	No use
Gate	Used to enable the counter operation (not necessary if gate force is used) (the operation is enabled when both external gate and soft-gate are ON)
EXT	No use
S1	No use
S2	No use

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Used to set the interval (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	No use
Hold value	H8007·H8006 / H800F·H800E	Stores the hold value (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled when both external gate and soft-gate are ON)
Output-enable	2 / 6	No use
Input-disable	3 / 7	Set to ON to disable count

(5) Operation

Instead of external pulses, PI232/272 counts its internal clock pulses. As the result, PI232/272 works as free-running timer in this mode.
The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

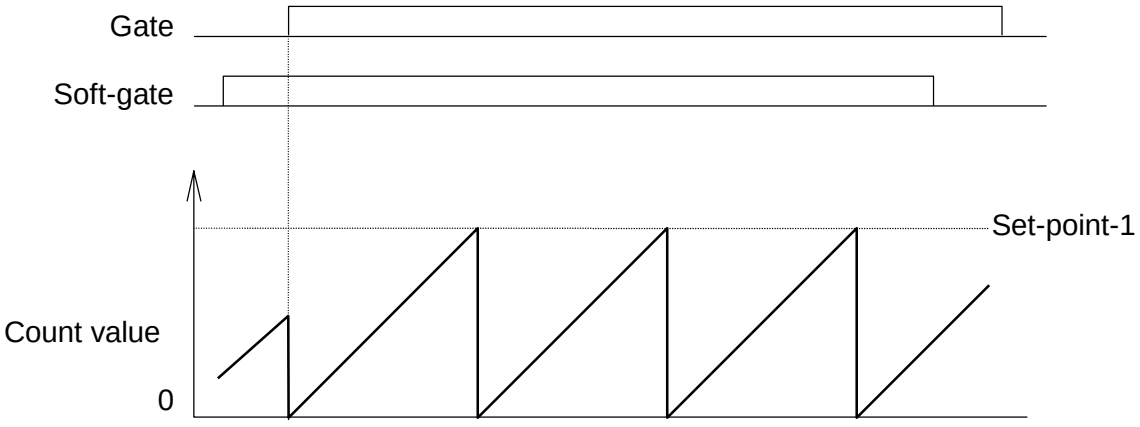
In the normal count mode, PI232/272 counts at the rising edge of the internal clock pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the internal clock pulse. The table below shows the time base which increases the count value by 1.

Count mode	Internal clock	Time base (= 1 count)
Normal	1 kHz	1 ms
	10 kHz	0.1 ms
	100 kHz	0.01 ms
Precision	1 kHz	0.5 ms
	10 kHz	0.05 ms
	100 kHz	0.005 ms

This mode function is enabled while both external gate and soft-gate are ON.
If the gate force function is used, this mode function is enabled by soft-gate ON.
(Note that when the gate condition is not fulfilled, the count value is no meaning)

When the count value reaches the set-point-1, the count value is reset to 0 (zero).
The set-point-1 can be set in the range of 1 to 16777215.

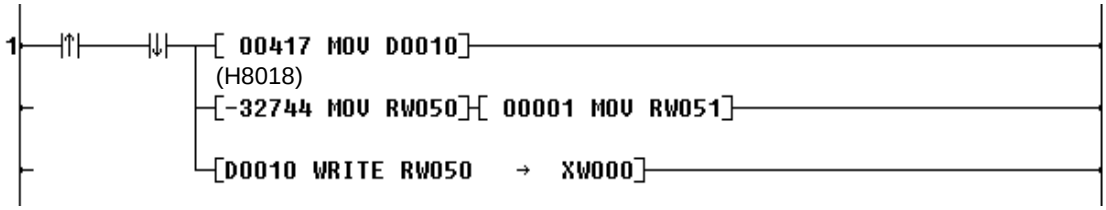
When the gate condition comes OFF, the current count value is transferred into the hold register.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

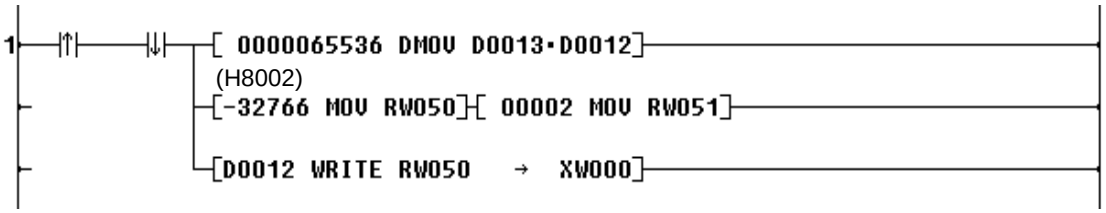
- Setting the programmable interval timer with 10 kHz clock for channel 1 (pulse mode = normal, gate force = forced)



At the beginning of RUN mode (at the second scan), the mode data 417 (H01A1) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

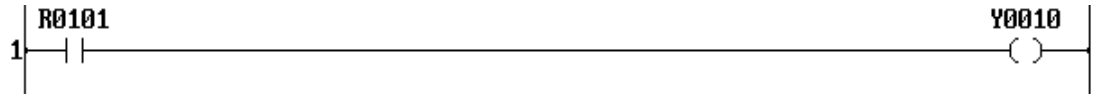
  Channel 1 Set-point-1 = 65536



At the beginning of RUN mode (at the second scan), the data 65536 is written into the addresses H8003·H8002 (CH1 set-point-1).

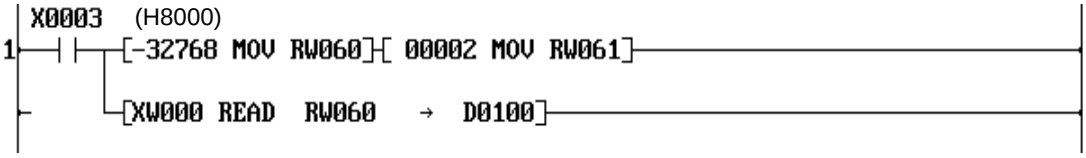
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON



When R0101 is ON, Y0010 is set to ON.

- Reading the count value



When X0003 (CH1 gate status) is ON, the count value is read and stored in the double-word register D0101·D0100.

6.7 Gate-ON timer mode

(1) Mode setting

Pulse count mode	Internal clock	Operation mode data
Normal	1 kHz	H0011 (17)
	10 kHz	H0021 (33)
	100 kHz	H0031 (49)
Precision	1 kHz	H0051 (81)
	10 kHz	H0061 (97)
	100 kHz	H0071 (113)

(2) External signals

Signal	Function
Phase A	No use
Phase B	No use
Marker	No use
Gate	Gate signal whose ON duration is measured
EXT	No use
S1	Hardware comparison output Comes ON when count value > set-point-1
S2	No use

(3) Buffer memory

Name	Address (CH1/CH2)	Function
Count value	H8001·H8000 / H8009·H8008	Stores the count value (read/write)
Set-point-1	H8003·H8002 / H800B·H800A	Can be used for hardware comparison output (read/write)
Set-point-2	H8005·H8004 / H800D·H800C	No use
Hold value	H8007·H8006 / H800F·H800E	Stores the count value in a gate ON duration (read only)
Mode	H8018 / H8019	Used to set the operation mode (write only)

(4) Command register (YW)

Name	Bit position (CH1/CH2)	Function
Soft-gate	0 / 4	Used to enable the counter operation (enabled while soft-gate is ON)
Output-enable	2 / 6	Set to ON to enable hardware comparison output
Input-disable	3 / 7	Set to ON to disable count

(5) Operation

PI232/272 measures the time duration of Gate signal ON state. The time is measured by counting PI232/272's internal clock pulses. The frequency of the internal clock can be selected from 1, 10 or 100 kHz.

In the normal count mode, PI232/272 counts at the rising edge of the internal clock pulse. On the other hand, in the precision count mode, PI232/272 counts at both rising and falling edges of the internal clock pulse. The table below shows the time base which increases the count value by 1.

The count rage is 1 to 16777215. The countable duration is also shown in the table.

Count mode	Internal clock	Time base (= 1 count)	Countable duration
Normal	1 kHz	1 ms	1 ms to 16777.215 s
	10 kHz	0.1 ms	0.1 ms to 1677.7215 s
	100 kHz	0.01 ms	0.01 ms to 167.77215 s
Precision	1 kHz	0.5 ms	0.5 ms to 8388.6075 s
	10 kHz	0.05 ms	0.05 ms to 838.86075 s
	100 kHz	0.005 ms	0.005 ms to 83.886075 s

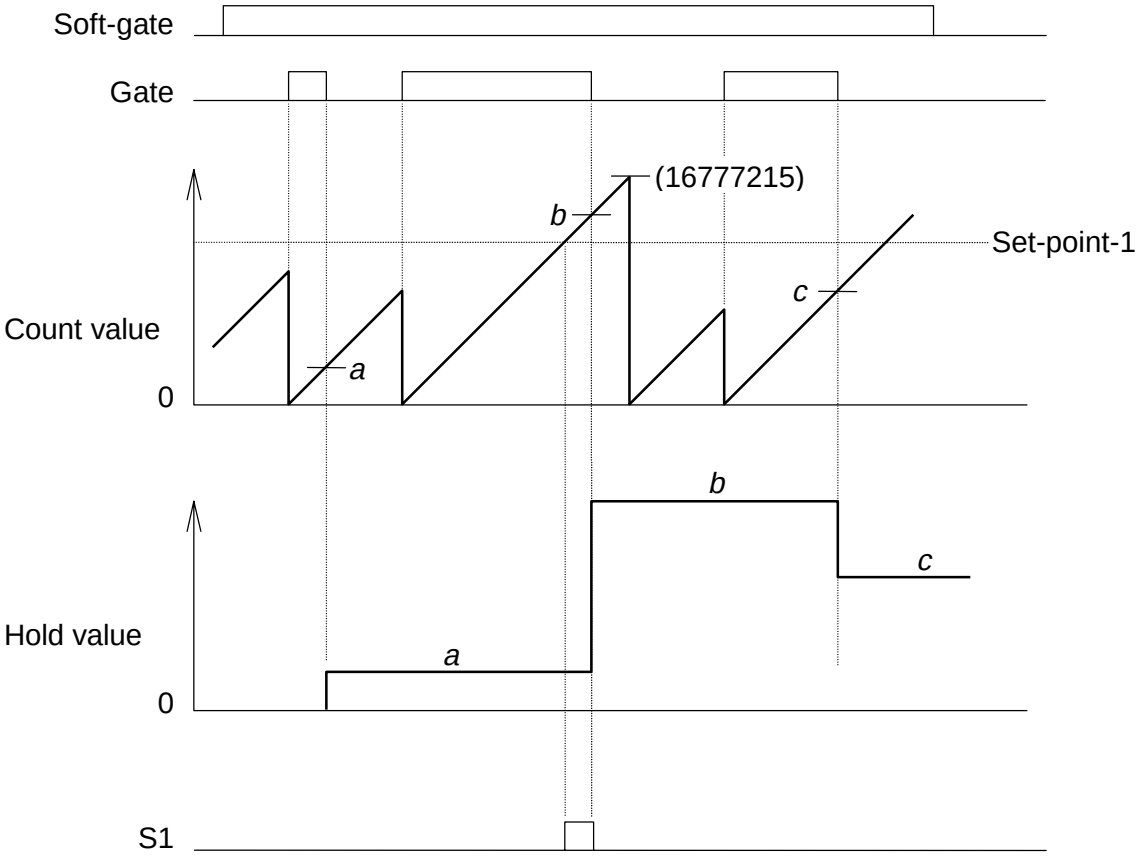
This mode function is enabled while soft-gate is ON.

When the Gate signal is changed to ON, the counting is started from 0. Then the Gate signal is changed to OFF, the count value is transferred to the hold register.

For example, if the hold register value is 7863 under the setting of 10 kHz precision mode, it means that the Gate ON duration was;

$7863 \times 0.05\ ms = 393.15\ ms$

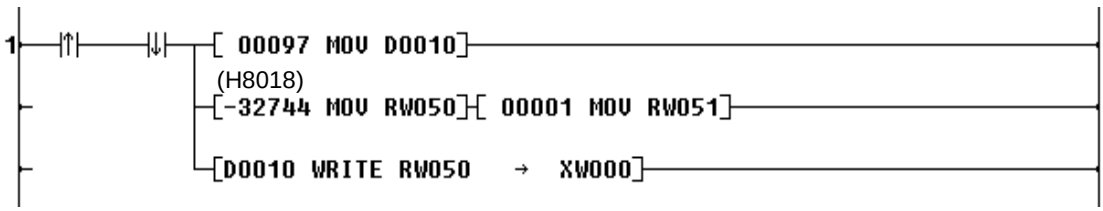
When the output-enable bit in the command register (YW) is ON, the hardware comparison output (S1) is enabled. In this condition, when the count value is greater than the set-point-1, S1 comes ON.



(6) Sample program

In the following sample programs, it is assumed that the PI232/272 is allocated to XW000 and YW001.

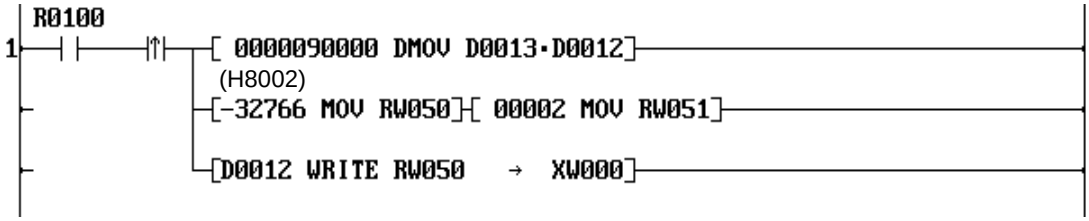
- Setting the gate-ON timer mode with 10 kHz clock for channel 1 (pulse mode = precision)



At the beginning of RUN mode (at the second scan), the mode data 97 (H0061) is written into the address H8018 (CH1 mode) of the buffer memory.

- Writing the set-point data

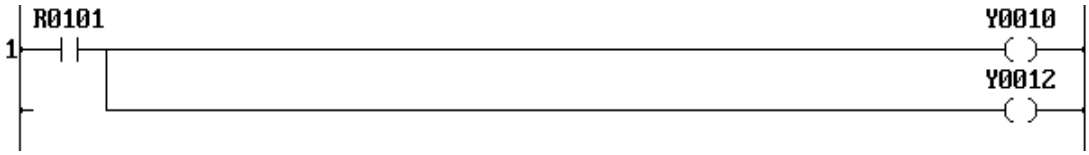
  Channel 1 Set-point-1 = 90000



  At the rising edge of R0100 coming ON, the data 90000 is written into the addresses H8003·H8002 (CH1 set-point-1).

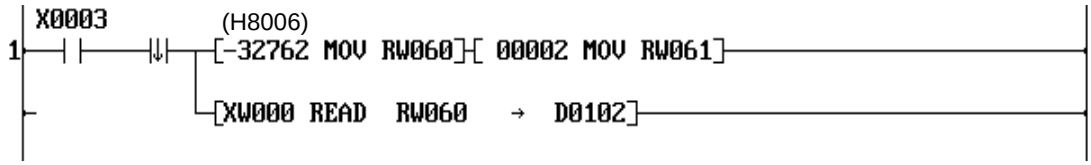
- Setting the command flags

  Channel 1 Soft-gate (Y0010) = ON
  Output-enable (Y0012) = ON



  When R0101 is ON, Y0010 and Y0012 are set to ON.

- Reading the hold value



  When X0003 (CH1 gate status) is changed to OFF, the hold value is read and stored in the double-word register D0103·D0102.

6. Function Details

Appendix

Appendix

A.1 Specification of the READ instruction

FUN 237 Special module data read (READ)
Reads designated range of data from the special module.
Input Execution output ———[A READ B → C]———

Function

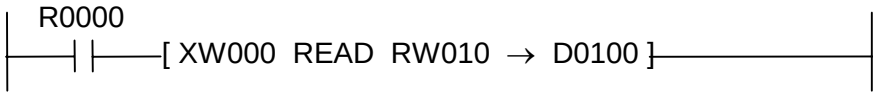
- This instruction reads data from the buffer memory of the special module that is designated by operand A, and stores them in T2's registers starting with operand C.
- The transfer source address (buffer memory address) is designated by operand B.
- The transfer size (number of words) is designated by operand B+1.

Input	Action	Output	ERF
OFF	No execution	OFF	
ON	Normal execution	ON	
	Error (see Note 2)	ON	ON

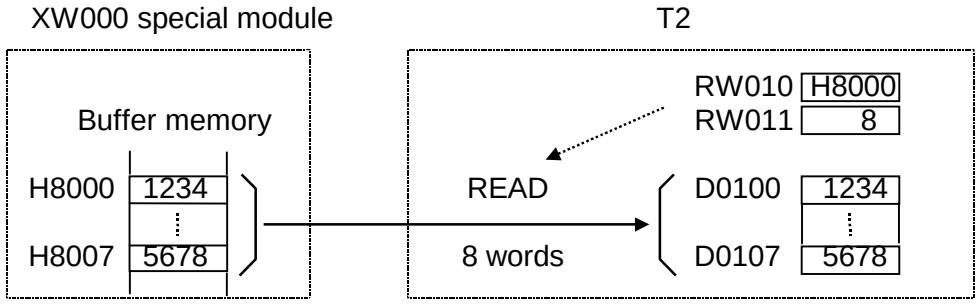
Operand

		Register															Constant	Index
Opr	Name	XW	YW	SW	LW	RW	W	T	C	D	F	IW	OW	I	J	K		
A	Special module	√	√														√	√
B	Transfer parameter	√	√	√	√	√	√	√	√	√	√							
C	Top register of destination		√	√	√	√	√	√	√	√	√							√

Program example

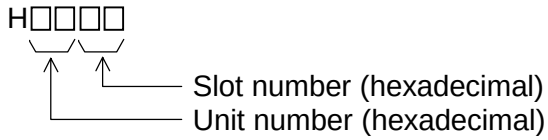


- When R0000 is ON, the buffer memory data of the size indicated by RW011, starting with the address indicated by RW010 of the special module allocated to XW000, are read and stored in D0100 and after.
- The maximum number of words to be read is 256 words. (16 words for PI232/272)



Note 1) The special module can be designated not only by the assigned register, but also by the mounting position. The mounting position is designated by a constant data for the operand A as follows.

(Unit number) × 256 + (Slot number)



Unit number	Hexadecimal
0	H00
1	H01
2	H02
3	H03

Slot number	Hexadecimal
0	H00
1	H01
2	H02
3	H03
4	H04
5	H05
6	H06
7	H07

For example, if a special module is mounted on Slot-4, Unit-0 (basic unit) and allocated to XW008 - YW09, the following two READ instructions are the same.

——[XW008 READ RW010 → D0100]——

——[H0004 READ RW010 → D0100]——

Note 2) The READ instruction is not executed as error in the following cases. In these cases, ERF (instruction error flag = S0051) is set to ON.

- When the operand A is other than a valid constant (see Note 1) or XW/YW register.
- When the designated special module has been disconnected.
- When no answer error occurs with the designated special module.
- When the number of words transferred exceeds 256 words.
- When the source table of transfer is out of the valid range.
- When the destination table of transfer is out of the valid range.

A.2 Specification of the WRITE instruction

FUN 238 Special module data write (WRITE)
Writes designated range of data into the special module.
Input Execution output ———[A WRITE B → C]———

Function

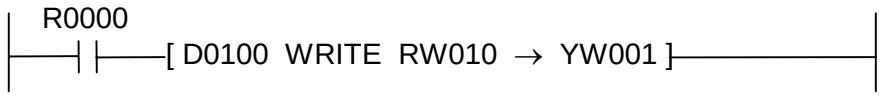
- This instruction transfers data stored in T2's registers starting with operand A into the buffer memory of the special module that is designated by operand C.
- The destination address (buffer memory address) is designated by operand B.
- The transfer size (number of words) is designated by operand B+1.

Input	Action	Output	ERF
OFF	No execution	OFF	
ON	Normal execution	ON	
	Error (see Note 2)	ON	ON

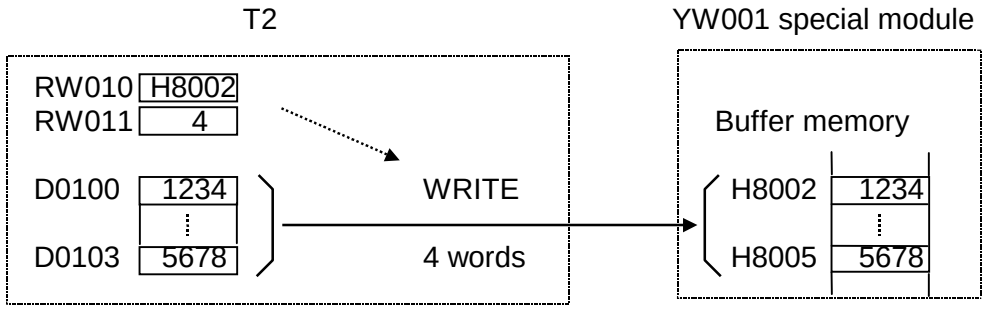
Operand

		Register															Constant	Index
Opr	Name	XW	YW	SW	LW	RW	W	T	C	D	F	IW	OW	I	J	K		
A	Top register of source	√	√	√	√	√	√	√	√	√	√							√
B	Transfer parameter	√	√	√	√	√	√	√	√	√	√							
C	Special module	√	√														√	√

Program example

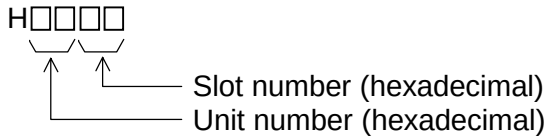


- When R0000 is ON, the register data of the size indicated by RW011, starting with D0100, are transferred to the buffer memory starting with the address indicated by RW010 of the special module allocated to YW001.
- The maximum number of words to be transferred is 256 words. (6 words for PI232/272)



Note 1) The special module can be designated not only by the assigned register, but also by the mounting position. The mounting position is designated by a constant data for the operand C as follows.

(Unit number) × 256 + (Slot number)



Unit number	Hexadecimal
0	H00
1	H01
2	H02
3	H03

Slot number	Hexadecimal
0	H00
1	H01
2	H02
3	H03
4	H04
5	H05
6	H06
7	H07

For example, if a special module is mounted on Slot-2, Unit-1 (expansion unit #1) and allocated to XW020 - YW021, the following two WRITE instructions are the same.

——[D0100 WRITE RW010 → XW020]——

——[D0100 WRITE RW010 → H0102]——

Note 2) The WRITE instruction is not executed as error in the following cases. In these cases, ERF (instruction error flag = S0051) is set to ON.

- When the operand C is other than a valid constant (see Note 1) or XW/YW register.
- When the designated special module has been disconnected.
- When no answer error occurs with the designated special module.
- When the number of words transferred exceeds 256 words.
- When the source table of transfer is out of the valid range.
- When the destination table of transfer is out of the valid range.

TOSHIBA

TOSHIBA CORPORATION
Industrial Equipment Department
1-1, Shibaura 1-chome, Minato-ku
Tokyo 105-8001, JAPAN
Tel: 03-3457-4900 Fax: 03-5444-9268