GaN MMIC for Ka-Band with 18W

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***Abstract*—A Ka-band high power amplifier MMIC developed from a robust process of 0.2μm gate-length AlGaN/GaN HEMT on SiC is presented. The MMIC chip was measured across 29 to 31GHz under pulsed bias condition. At VDD=28V, The MMIC chip achieved a power added efficiency of 17% with an output power of 18W. The 2-stage amplifier GaN MMIC has 10.2dB linear gain and a die-size of 4.0mm x 5.5mm. The MMIC can realize high power Solid-State Power Amplifier.**

Keywords—Gallium Nitride, MMIC, power amplifiers, millimeter wave

I. Introduction

In recent year, the Travelling-Wave Tube Amplifier (TWTA) has being replaced by Solid-State Power Amplifier (SSPA) using GaN devices, because GaN devices have high power, high gain and high efficiency. Interest has also moved to higher frequencies. For Ka-band satellite communication (SATCOM) market, the emergence of GaN HEMT devices with promising performances at millimeter-wave [1] – [5] has drawn a great deal of research interests in high power amplifier at Ka-band. Many of the high gain GaN MMICs demonstrated has a relatively low output power of about 5W or less [6] – [10], and only in recent year reached a high 9W [10] – [12].

To realize a 100W SSPA using 9W MMICs, it would require more than 12 components and this would cause a loss of power at the dividing and combining. While with a MMIC of 18W output power the required number of component can be reduced to 6 and the loss of power at the dividing and combining can also be improved. We had reported a 2-stage GaN MMIC for Ka-band with 20W of output power, but the power added efficiency was 16%.

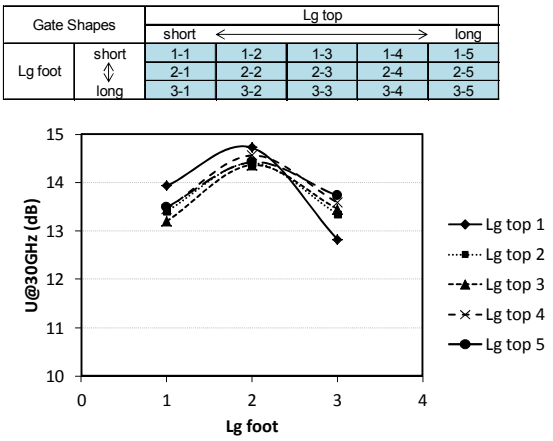
In this paper, robustness for fabrication of the MMIC is presented. To examine robustness for fabrication, we made TEG (Test Element Group) matrix which was five levels of top length of gate by three levels of foot length of gate. And the 2-stage GaN MMIC amplifier was optimized to efficiency. Then it shows an output power of 18W with 19% of PAE at 31GHz.

II. Device Technology

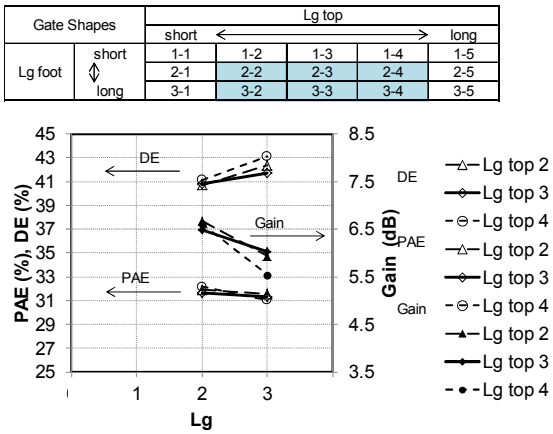
The device used in the MMIC design was based on a AlGaN/GaN HEMT process of 0.20μm gate length technology. The heterostructure was formed from an $Al_{0.3}Ga_{0.7}N$/GaN epitaxial layer that was grown by metal-organic chemical vapor deposition (MOCVD) on a SiC substrate. Isolation between devices was achieved through mesa etch using a reactive-ion etch (RIE) process. The source and drain ohmic contacts which comprises of Ti/Al metal stack were formed using rapid thermal annealing (RTA). The Y-shaped gate was defined by electron-beam lithography and its Schottky contact was constructed using Ni/Au metal stack. The passivation layer of Si_3N_4 film was deposited on the surface of AlGaN and the gate metal through plasma-enhanced chemical vapor deposition (PE-CVD). The interconnections including air-bridges were formed through Au-plating. After the front-side processing, the wafer was thinned to 50μm by mechanical polishing and via-holes were dry-etched through the substrate using an inductively-coupled -plasma (ICP) etcher. The back-side of the wafer was galvanized with gold metallization for the grounding.

In order for the GaN device to achieve optimal performances at millimeter-wave frequencies, special attentions were paid to the formation of the epitaxial layer structure, the gate fabrication techniques and the layout pattern. The device had 50um of thickness and four via-holes at the source terminal to reduce its parasitic inductance to the ground plane [2].

Before starting circuit design, we examined influence with the gate shape in the RF performance. One of the gate shape parameters is top length of gate which has influence for the gate resistance and the capacitance between the gate and the drain. We made five levels from -20% to +80%. Another parameter is the foot length of gate which has influence for the gate capacitance and transconductance. We made five levels from -50% to +50%. Fig. 1 shows the Mason's U of a 50μm gate-width 8-finger FET cell for fifteen types of TEG. U had a peak at center level of the foot length of gate. It means that the shorter foot length of gate made short channel phenomena which causes the transconductance smaller and that the longer foot length of gate made the gate capacitance lager. U didn't show dependency for the top length of gate. It means the gate resistance and the capacitance are small enough. Fig. 2 shows the MSG/MAG and Mason's U of a 50μm gate-width 8-finger FET cell 2-2. Extrapolating the curves of Mason's U with a slope of -6dB/octave, the figure-of-merit fmax was estimated to be 135GHz. The current gain decays with frequency with a slope of -6dB/octave. The current-gain cutoff frequency fT is 33 GHz.



(a) S-parameter measurements



(b) Loadpull measurements

Fig. 1 Gate length dependency of (a)Mason's U and (b) PAE of unit FET cells with 50μm-8-finger

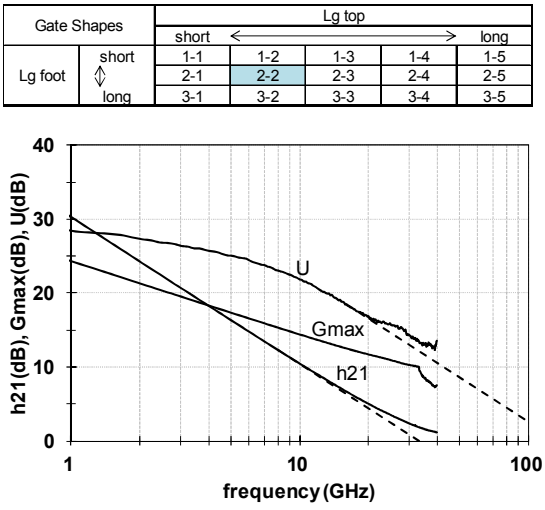


Fig. 2 h21, Gmax and Mason's U of the unit FET cells with 50μm-8-finger of Lg_top=type2/Lg=type2

III. Loadpull Characteristics

Loadpull measurement was performed on the FET cell to determine the optimum load impedance using a passive-tuner system at 31GHz. However, at millimeter-wave frequencies, there was a limit on the VSWR range that can be measured by the tuner. This affects in particularly low impedance device that may exhibit optimum impedance terminations at outside of the measurable VSWR range. In this work, a pre-match circuit was incorporated into the FET cell to transform its impedance to within the VSWR range that could be evaluated by the passive-tuner. The real impedance of the FET cell was then obtained by de-embedding the pre-match circuit.

A 50μm×8 FET cell biased at VDD=24V was evaluated at 31GHz. In Fig. 3, the broken line shows the limit of the VSWR range that can be measured by the tuner and solid lines show the output power contour lines of the FET cell with pre-match circuit. Γ_{PMFET} at the center of the contour lines is the optimum load impedance for output power of the FET cell with pre-match circuit.

Fig. 4 shows the drain efficiency (DE), gain and PAE of a 50μm gate-width 8-finger FET cell for six types of TEG when PAE shows the peak. The longer foot length of gate showed higher DE than the shorter. The shorter foot length of gate showed higher gain than the longer. As the result, PAE didn't show dependency for the foot length of gate. As similar to U, the gate length was robust enough for DE and gain.

Fig 5 shows the results of loadpull measurements for 50μm gate-width 8-finger FET cell 2-2 and 3-2. The FET cell which had a longer foot length of gate achieved a saturated output power of 32.0dBm (4.0W/mm) with 45% of peak DE and 31.6% of peak PAE. The FET cell which had a shorter foot length of gate achieved a saturated output power of 31.7dBm (3.7W/mm) and 31.9% of peak PAE. Because the PAE of both was almost the same and the shorter foot length of gate showed higher gain, the shorter foot length of gate was selected for the target structure of the gate.

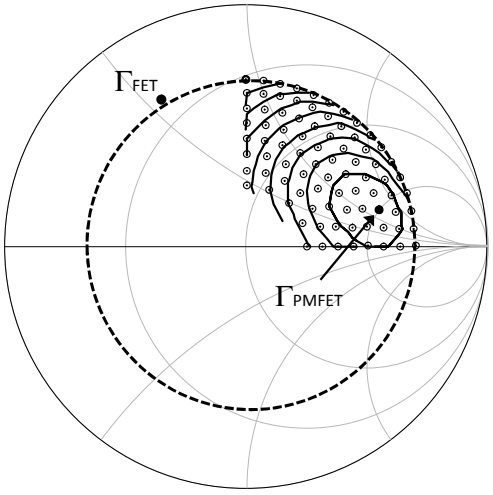


Fig. 3 Loadpull impedance of FET cell with pre-match circuit (Γ_{PMFET}) and its de-embedded impedance (Γ_{FET})

Gate Shapes		Lg top				
		short ⟷				long
Lg foot	short ⇕ long	1-1	1-2	1-3	1-4	1-5
		2-1	2-2	2-3	2-4	2-5
		3-1	3-2	3-3	3-4	3-5

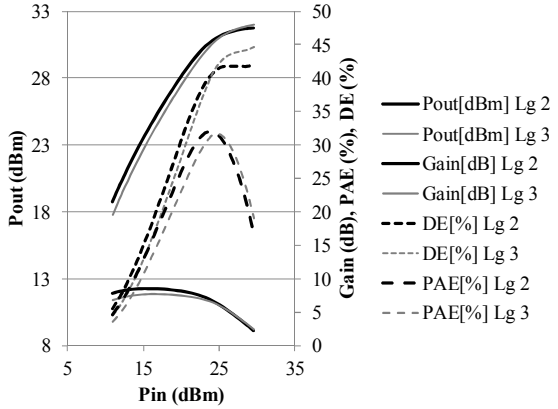


Fig. 4 Loadpull results of FET cell at 31GHz

IV. Circuit Design

Using the 50µm×8 FET cell as the basic cell, a 2-stage design was implemented to achieve a targeted gain of 11dB and an output power of 18W. Fig. 5 illustrates the block-diagram of the 2-stage MMIC. With a power-density of 3.3W/mm, the gate-width of the output amplifier stage was calculated as 6.4mm to meet the power specification. This corresponds to a 16 FET cells for an output power stage which was driven by an 8 FET cells for a driver stage (3.2mm). A staging ratio of 2:1 between the amplifier stages results in a good PAE versus bandwidth performance [13] while ensuring enough driving capability at the driver stage.

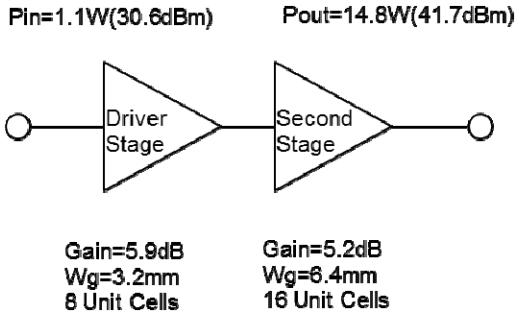


Fig.5 Block diagram of the 2-stage MMIC

The MMIC was designed to operate in Class-AB mode and reactively matched. Both the driver and the output power stage were matched to the measured loadpull impedance modeled by the RC equivalent circuit scaled to their required gate-width periphery. The matching networks were designed across a 12% bandwidth so as to meet the design goal with process variations. All the devices were made unconditionally stable by adding an RC-network in series with the gate ports, however, this reduced the linear gain of the MMIC by 2dB. Odd-mode oscillations were analyzed [14] and suitable resistors were added to both the gate and drain to avoid the oscillation. Stability was checked and ensured at the device, each individual amplifier stages and the full MMIC.

The circuits were simulated using Agilent's ADS and the coupling of the transmission lines at the matching networks was verified with extensive EM simulation. Fig. 6 shows the microphotograph of the fabricated GaN MMIC which measures 4.0mm×5.5mm.

V. Measurement Results

For this initial evaluation step, the MMIC samples were measured on-wafer across 29GHz to 31GHz under pulsed bias condition to avoid thermal affect.

At VDD=24V, the MMIC achieved a PAE of 17.4% and a saturated output power of 41.9dBm (15.5W) at 31GHz. The MMIC had a linear gain of 10.1dB and while driven into saturation, it had an associated power gain of more than 6.1dB and drain efficiency of more than 22.5%. Fig. 7(a) shows the measured output power, efficiency and gain of the MMIC during saturation output power at VDD=24V.

At VDD=28V, the MMIC achieved a PAE of 17.4% and a saturated output power of 42.6dBm (18.2W) at 31GHz. The MMIC had a linear gain of 10.7dB and while driven into saturation, it had an associated power gain of more than 6.8dB and drain efficiency of more than 21.7%. Fig. 7(b) shows the measured output power, efficiency and gain of the MMIC during saturation output power at VDD=28V.

Fig.9 benchmarks this work with the published Ka-band GaN high power amplifier MMIC of 2-stages or more. It can be seen that the developed MMIC only achieved more than 15W as the highest output power performance. However, when compared to the other state-of-the-art MMIC, it has a lower gain and efficiency.

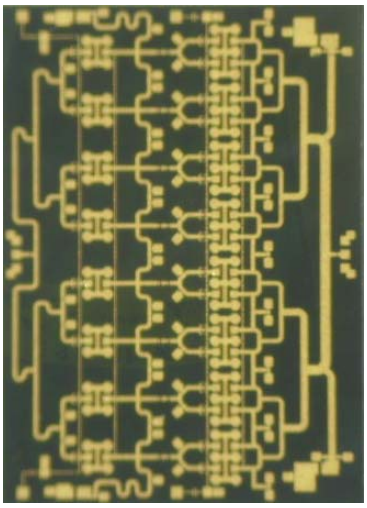
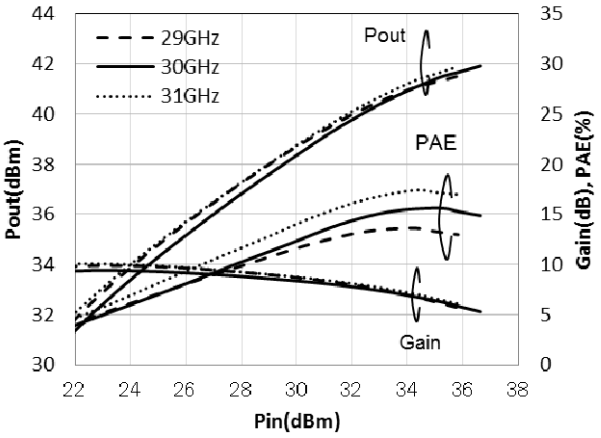
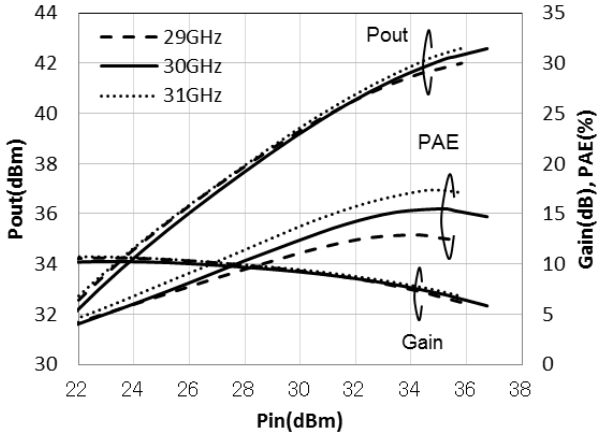


Fig. 6 Microphotograph of the developed GaN MMIC



(a) VDD=24V



(b) VDD=28V

Fig. 7 Measured power, efficiency and gain with swept input power at (a) VDD=24V and (b) VDD=28V

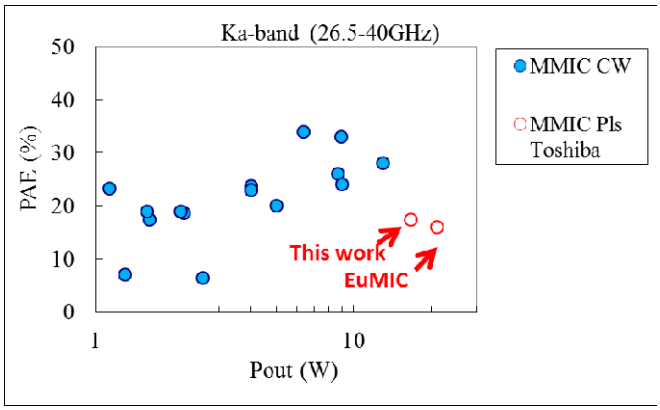


Fig. 8 PAE of GaN MMIC for Ka-band versus Pout.

VI. Conclusion

A high-power MMIC developed from in-house 0.20μm gate-length GaN HEMT process is demonstrated at Ka-band. Under pulsed bias condition at VDD=28V, the MMIC achieved a saturated output power of 18W at 31GHz. The influence with the gate shape in the RF performance is small enough for our process control. To improve the efficiency, we should reduce the loss in the circuit more. This MMIC will be expected to further enhance Ka-band SATCOM systems' performance in terms of higher output power and smaller size.

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