A 2 W 45 % PAE X-Band GaN HEMT Class-F MMIC Power Amplifier

Tomohiro Senju [1], Kazutaka Takagi [2], Hideki Kimura [3]

Komukai Complex, Toshiba Infrastructure Systems & Solutions Corporation
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Kanagawa, 212-8581, Japan
[1]tomohiro.senju.rf@toshiba.co.jp
[2]kazu.taka.yk@toshiba.co.jp
[3]hideki3.kimura.uu@toshiba.co.jp

***Abstract* — Applying a 0.25 μm GaN HEMT MMIC technology and a class-F harmonic tune technique, a design of a small-sized high-efficiency 2 W X-band MMIC power amplifier is presented. The fabricated MMIC power amplifier exhibits the output power of 32.7-33.3 dBm and the PAE of 41-45 % at Vds = 30 V under pulse operation of duty of 10% in the frequency range of 8.8-9.8 GHz, which are in good agreement with simulated results.**

Index Terms — PAE, X-band, GaN HEMT, class-F, power amplifiers, MMICs (key words)

I. Introduction

For transmitter circuits and their peripheral circuits, which are used in the front end of X-band AESA systems mounted on the aircraft, smaller size and higher efficiency are strongly required in terms of lower costs and smaller system size. High output power amplifiers (HPAs) occupy a very large area in output stages of transmitter circuits, and development of highly integrated and highly efficient HPAs is rapidly progressing due to recent GaN MMIC technology advances.

Several high efficiency 10-43 W class GaN MMIC HPAs for X-band AESA systems have been reported [1]-[3], and their power gains are approximately 13-20 dB, which means 0.1-2 W class driver amplifiers (DAs) are required in front of HPAs. As DAs, Low-cost, wide-band GaAs MMIC power amplifiers (PAs) are widely used [4]. However, GaAs MMIC PAs are often biased with a voltage range of 3-10 V, whereas GaN HPAs with a voltage range of 20-30 V, which means two types of bias circuits for both DAs and HPAs are required and leads to the enlargement of the peripheral circuit.

To simplify the peripheral circuit, applying a GaN HEMT technolgy to a DA is a good choice because of using a common operating voltage for both HPAs and DAs. It is also easy to achieve high-efficiency operation with a harmonic tuning technique due to high-voltage characteristics of GaN HEMTs.

Output fundamental frequency impedance of younger stage FETs in multistage 10-40 W class HPAs is several ohms, whereas that of multistage 2 W class DAs is much higher than 50 ohms. Therefore, it becomes more critical to achieve broad band and low loss inter-stage matching network design in multistage 2 W class DAs than that in 10-40 W class HPAs because of much increase in the ratio of impedance transformation between inter-stages.

In this paper, a PAE optimal output matching circuit topology for 2 W X-band class-F amplifier is first examined from comparison among several circuit topologies in terms of minimizing circuit loss and maximizing band width. Then a PAE optimal inter-stage matching circuit topology is decided by considering carefully the balance between fundamental frequency circuit loss and FET's drain efficiency of each stage.

Finally a high-efficiency 2 W X-band 3-stage GaN MMIC DA is designed and fabricated. Consequently, an output power of 32.7-33.3 dBm and a PAE of 41-45 % at operating voltage 30 V are obtained from measurement in the frequency range of 8.8-9.8GHz, which are in good agreement with those calculated from nonlinear circuit simulations.

II. Technology

We adopt a 0.25 μm GaN HEMT technology for this X-band amplifier. The device exhibits the high-frequency performance of fmax ≥ 90 GHz for a unit FET with a gate width of 4x100 μm, and it has a breakdown voltage of greater than 100 V, a maximum drain current of 1 A/mm, and a power density of greater than 4 W/mm with a drain voltage (Vds) of 30 V and a drain current (Idq) of 83 mA/mm.

A unit amplifier consists of a GaN HEMT and a parallel RC network, which is connected in series to the gate terminal of the active device to avoid oscillation. Optimum harmonic impedance required for the class-F amplifier design operating at 9.3 GHz was calculated through harmonic load pull simulations with a nonlinear transistor model in order to obtain a maximum PAE in the vicinity of saturated output power as shown in Table I.

TABLE I

PAE Optimum Source/Load Impedance

Z_s_fund	9.1 + j*57.0
Z_s_2nd	1.4 + j*21.7
Z_l_fund	51.7 + j*99.3
Z_l_2nd	1.5 - j*20.2
Z_l_3rd	3.1 + j*59.5

Figure 1 shows the calculated output power and PAE characteristics of the unit amplifier with the class-F impedance condition. A PAE of 66 % and an output power of 33.1 dBm are yielded with an input power of 25 dBm.

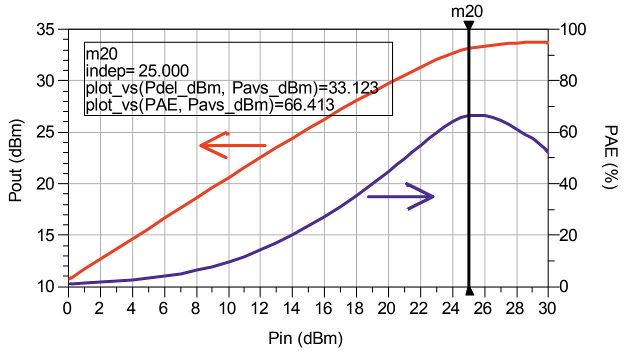


Fig. 1. Simulated output power and PAE results of a 9.3 GHz Class-F GaN HEMT unit amplifier with a Vds of 30 V.

III. Power Amplifier Design

A. *Design of an Multi-stage Power Amplifier Configuration*

Table II shows the 2 W X-band MMIC PA target performance. To achieve the performance, a power budget for the MMIC PA was calculated as shown in Fig. 2.

TABLE II

Target Performance

Supply Voltage (V)	30
Frequency (GHz)	8.8 - 9.8
Gain (dB)	20 (typ.)
Output Power (dBm)	33 (typ.)
PAE (%)	45 (typ.)

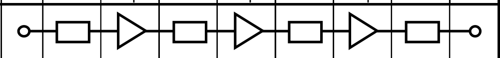
	RFin	MN in	Unit Amp1	MN 1-2	Unit Amp2	MN 2-3	Unit Amp3	MN out	RFout	Total
										
Gain or Loss(dB)		-1.5	9.0	-1.5	8.5	-1.5	8.0	-0.4		20.6
Power(dBm)	12.4	10.9	19.9	18.4	26.9	25.4	33.4	33.0	33.0	33.0
Pdc(W)			0.4		1.0		3.0			4.4
PAE(%)			23.1		41.6		61.1			45.0
Drain Eff.(%)			26.5		48.5		72.5			
Pdiss(W)			0.3		0.6		1.2			2.0

Fig. 2. A power budget for a 2W X-band GaN MMIC PA.

Defining an output stage amplifier as the 3rd stage unit amplifier with the output matching network in the Fig. 2, the PAE of the output stage amplifier (PAE3) is obtained from the PAE and the power gain of the 3rd stage unit amplifier (PAE3u, Gp3_dB) and the output matching network insertion loss (Loss_dB) as:

$$\mathrm{PAE3} = \mathrm{PAE3u} \times \left[1 - \frac{10^{\left(\frac{Gp3\_dB}{10}\right)}}{10^{\left(\frac{Gp3\_dB}{10}\right)} - 1} \times \left\{1 - 10^{\left(\frac{-Loss\_dB}{10}\right)}\right\}\right] . \quad (1)$$

In reference to Fig. 2, PAE3 is found to be 54.7 % by substituting PAE3u = 61.1 %, Gp3_dB = 8 dB, and Loss_dB = 0.4 dB to (1).

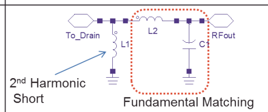
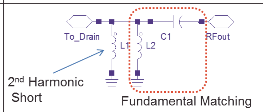
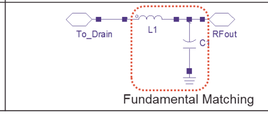
B. *Design of an Output Matching Network*

Considering a fundamental output matching network along with or without a class-F harmonic tuning network for the output stage amplifier, output matching network configuration shown as type 1 to 3 in Table III are considered as candidates.

The configuration of type 1 exhibits a moderate insertion loss of 0.45 dB but the highest PAE of 55.9 % among them due to the harmonic tuning, which is most suitable for this MMIC PA target. Then type 2 exhibits a slightly greater insertion loss than that of type 1, because shunt inductances used for a fundamental matching consist of the lossy transmission lines. On the other hand, the simplicity of type 3 can help to reduce the insertion loss, but the lack of the harmonic tuning circuit restricts to a lower PAE than that of type 1.

TABLE III

Comparison of Various Output Matching Networks

No	Description	Schematic	Output Port Return Loss Of MNout (dB)	Insertion Loss of MNout (dB)	PAE (%)
1	LPF- type Fundamental Matching w/ Harmonic Tuning		25	0.45	55.9
2	HPF- type Fundamental Matching w/ Harmonic Tuning		18	0.52	52.2
3	LPF- type Fundamental Matching w/o Harmonic Tuning		18	0.24	53.9

C. *Design of a Three-Stage Power Amplifier Circuit*

Circuit parameters of type 1 output matching network are designed using a commercial circuit simulator to put the network impedance close to the class-F optimum impedance in Table I. After that, circuit parameters of an input matching network with almost the same circuit configuration as the output are designed in the same manner. Because using a harmonic tuning circuit for the inter-stage decreases the efficiency due to the circuit loss increase in the fundamental frequency band, only the fundamental matching is adopted for the 1st and 2nd stage unit amplifier.

After individually designed each stage unit amplifier with matching circuits is connected in series, parameters of each matching circuit are adjusted so that the output power and PAE in the frequency band of 8.8 to 9.8 GHz should be flattened.

Finally considering the effects of parasitic components in the layout pattern through electromagnetic simulation, the circuit parameters are readjusted so that the output power and the PAE in the band to be flattened.

IV. Fabricated Results

A photograph of the fabricated GaN MMIC PA is shown in Fig. 3 and the chip occupies an area of 2.0 mm x 3.1 mm.

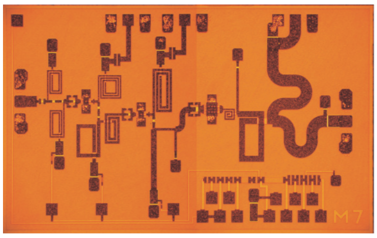
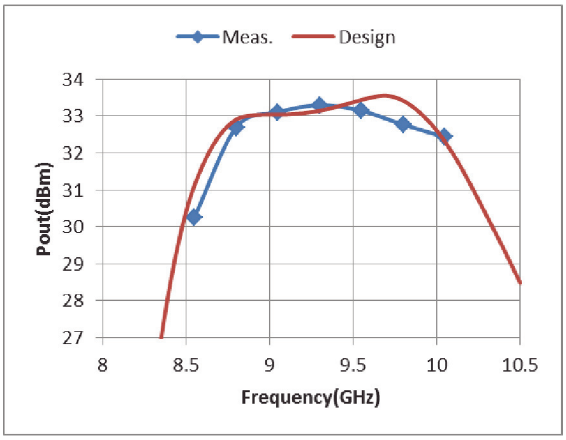
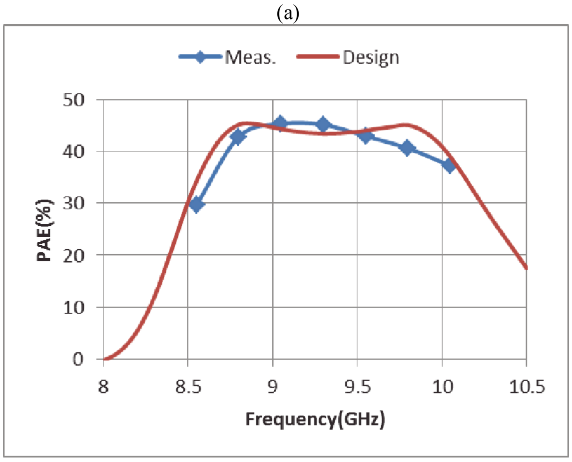


Fig. 3. Photograph of 2 W X-band GaN MMIC PA. The chip size is 2.0 mm x 3.1 mm.

Figure 4 shows a comparison between the designed and measured performances of the GaN MMIC PA under pulse operation of duty of 10%, which shows good agreement. The measured ouput power of 32.7-33.3 dBm and the PAE of PAE 41-45 % are obtained.



(a)



(b)

Fig. 4. Measured Pout and PAE results of 2 W X-band GaN MMIC PA with Vds = 30 V under pulse operation of duty of 10% and Pin = 15 dBm. : (a) Pout; (b) PAE

From Table IV, to our knowledge, one of the world's highest efficiency for 1-2 W class X-band GaAs/GaN MMIC PAs with more than 10 dB power gain is found to be realized through this work.

TABLE IV

Comparison Between 1-2 W Class X-Band GaAs/GaN MMIC PAs

Ref	Technplogy	Frequency (GHz)	Saturated Output Power (dBm)	Power Gain (dB)	PAE (%)	Drain Voltage (V)	Operation Mode
This work	GaN HEMT (0.25um)	8.8-9.8	32.7-33.3	17.7-18.3	41-45	30	Pulse D.C.=10%
[5]*	GaAs pHEMT (0.25um)	9-10	30	20	30	9	CW
[6]*	GaAs pHEMT (0.25um)	9-10	32	18	37-41	8	Pulse D.C.=10%
[7]*	GaAs	9-10	32.5-33	14.5-15	35-37	8	CW
[8]*	GaN HEMT (0.25um)	9-10	33.0-34.5	14.0-15.5	31-37	20-30	CW
[9]	GaN HEMT (0.3um)	8-12	32.5	13	8	35	Pulse D.C.=10%

*Commercial Product

V. Conclusion

Applying the GaN MMIC technology and the class-F harmonic tune techniques, a small-sized high-efficiency 2 W X-band driver amplifier suitable for the transmit module of AESA system was designed and fabricated. The output power of 32.7-33.3 dBm and the PAE of 41-45 % at operating voltage 30 V in the frequency range of 8.8-9.8 GHz were achieved, which were in good agreement with the calculated results obtained through circuit simulations with nonlinear GaN HEMT models.

Acknowledgment

The authors would like to thank Mr. K. Tahara for his continuous support through circuit designs and evaluations.

References

[1] S. Piotrowicz, Z. Ouarch, E. Chartier, R. Aubry, G.Callet, D. Floriot, J.C.Jacquet, O. Jardel, E. Morvan, T. Reveyrand, N. Sarazin, and S.L. Delage, "43W, 52% PAE X-Band AlGaN/GaN HEMTs MMIC Amplifiers," *IEEE MTT-S Digest*, pp. 505 – 508, May 2010.

[2] C. Costrini, M. Calori, A. Cetronio , C. Lanzieri , S. Lavanga , M. Peroni , E. Limiti, A. Serino, G. Ghione, and G. Melone, "A 20 Watt Micro-strip X-Band AlGaN/GaN HPA MMIC for Advanced Radar Applications," in European Microwave Conference Proceedings, 2008, pp. 1433 – 1436.

[3] "CMPA801B025D data sheet," Wolfspeed, 2010.

[4] S. Masuda, M. Yamada, T. Ohki, K. Makiyama, N. Okamoto, Y. Nakasha, K. Imanishi, T. Kikkawa, and H. Shigematsu, "C-Ku Band GaN MMIC T/R Frontend Module Using Multilayer Ceramics Technology," *IEEE MTT-S Digest*, June 2011.

[5] "TGA2700 data sheet," Qorvo, 2009.

[6] "CHA6005-99F data sheet," UMS.

[7] "MAAM71100 data sheet," M/A-COM.

[8] "TGA2598 data sheet," Qorvo, 2015.

[9] P. Schuh, R. Leberer, H. Sledzik, M. Oppermann, B. Adelseck, H. Brugger, R. Quay, M. Mikulla and G. Weimann, "Advanced High Power Amplifier Chain for X-Band T/R-Modules based on GaN MMICs," in European Microwave Conference Proceedings, 2006, pp. 241 – 244.