A 20-Watt Ka-Band GaN High Power Amplifier MMIC

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Abstract—**A Ka-band high power amplifier MMIC developed from 0.18μm gate-length AlGaN/GaN HEMT on SiC is presented. The MMIC chip was measured on-wafer across 29GHz to 31GHz under pulsed bias condition. At VDD=28V, the MMIC achieved an output power of 19W to 21W. To the authors' best knowledge, this is the highest output power ever reported for GaN high power amplifier MMIC at Ka-band. The 2-stage amplifier GaN MMIC has 10dB linear gain and a die-size of 4.0mm x 5.5mm. The MMIC can realize high power Solid-State Power Amplifier (SSPA) for Ka-band.**

Keywords—Gallium Nitride, MMIC, power amplifiers, millimeter wave

I. INTRODUCTION

The Travelling-Wave Tube Amplifier (TWTA) is being replaced by Solid-State Power Amplifier (SSPA) using GaAs devices, because GaAs devices have excellent reliability and can minimized the size of SSPA. For Ka-band satellite communication (SATCOM) market, the emergence of GaN HEMT devices with promising performances at millimeter-wave [1] – [4] has drawn a great deal of research interests in high power amplifier both in MMICs and discrete amplifiers at Ka-band. One of these excellent characteristics is high output power. We had developed a pre-match GaN HEMT device with an output power of 18W at 31GHz [5]. However, because the device is a discrete amplifier designed with one amplifier stage, it has limited gain and bandwidth. On the other hand, many of the high gain GaN MMICs demonstrated have a relatively low output power of about 5W or less [6] – [10], and only in recent years reached a high 11W [11] – [13].

To realize a 100W SSPA using 9W MMICs, it would require more than 12 components and this would cause a loss of power at the dividing and combining components. While with a MMIC of 18W output power the required number of component can be reduced to 6 and the loss of power at the dividing and combining can also be improved. In this paper, a 2-stage GaN MMIC amplifier with an output power of 19W to 21W across 29GHz to 31GHz is presented. To the authors' best knowledge it is the highest output power ever demonstrated for GaN power amplifier MMIC across this frequency band. This power capability makes it attractive for use in SSPA for Ka-band SATCOM applications.

II. DEVICE TECHNOLOGY

The device used in the MMIC design was based on a AlGaN/GaN HEMT process of 0.18μm gate length technology. The heterostructures was formed from an $Al_{0.3}Ga_{0.7}N$/GaN epitaxial layer that was grown by metal-organic chemical vapor deposition (MOCVD) on a SiC substrate. Isolation between devices was achieved through mesa etch using a reactive-ion etch (RIE) process. The source and drain ohmic contacts which comprises of Ti/Al metal stack were formed using rapid thermal annealing (RTA). The Y-shaped gate was defined by electron-beam lithography and its Schottky contact was constructed using Ni/Au metal stack. The passivation layer of Si_3N_4 film was deposited on the surface through plasma-enhanced chemical vapor deposition (PE-CVD). The interconnections including air-bridges were formed through Au-plating. After the front-side processing, the wafer was thinned to 50μm by mechanical polishing and via-holes were dry-etched through the substrate using an inductively coupled plasma (ICP) etcher. The back-side of the wafer was galvanized with gold metallization for the grounding.

In order for the GaN device to achieve optimal performances at millimeter-wave frequencies, special attentions were paid to the formation of the epitaxial layer structure, the gate fabrication techniques and the layout pattern. The device had four via-holes at the source terminal to reduce its parasitic inductance to the ground plane [2]. Fig. 1 shows the MSG/MAG and Mason's U of a 50μm gate-width 8-finger
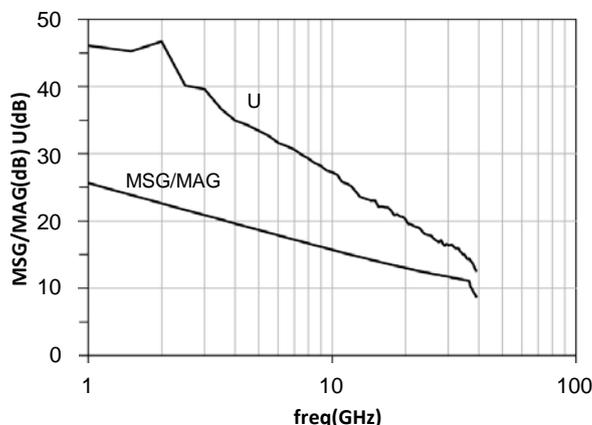
Fig. 1 MSG/MAG and Mason's U of the 50μm gate-width 8-finger FET cell

FET cell. Extrapolating the curves of Mason's U with a slope of -20dB/decade, the figure-of-merit fmax was estimated to be 110GHz. DC characteristics of the device were saturation current Idss=820mA/mm, transconductance gm=400mS/mm at Vds=5V and a pinch-off voltage=-2V.

III. Loadpull Characteristics

Loadpull measurement was performed on the FET cell to determine the optimum load impedance using a passive-tuner system at 31GHz. However, at millimeter-wave frequencies, there was a limit on the VSWR range that can be measured by the tuner. This affects in particularly low impedance device that may exhibit optimum impedance terminations at outside of the measurable VSWR range. In this work, a pre-match circuit was incorporated into the FET cell to transform its impedance to within the VSWR range that could be evaluated by the passive-tuner. The real impedance of the FET cell was then obtained by de-embedding the pre-match circuit.

At first, a 50µm×8 FET cell biased at VDD=24V was evaluated at 31GHz. In Fig. 2, the broken line shows the limit of the VSWR range that can be measured by the tuner and solid lines show the output power contour lines of the FET cell with pre-match circuit. Γ_{PMFET} at the center of the contour lines is the optimum load impedance for output power of the FET cell with pre-match circuit. And Γ_{FET} at just outside the measurable VSWR range is the optimum load impedance of the de-embedded FET cell. After de-embedding, the optimum load impedance tuned for maximum output power was found to be 11.6 + j27.7 ohm. At this impedance, the FET cell achieved a saturated output power of 31.2dBm (3.3W/mm), an associated gain of 7dB and PAE of 40% as shown in Fig. 3. The de-embedded load impedance was modeled using a simple RC equivalent circuit for matching network synthesis across frequency in the circuit design.
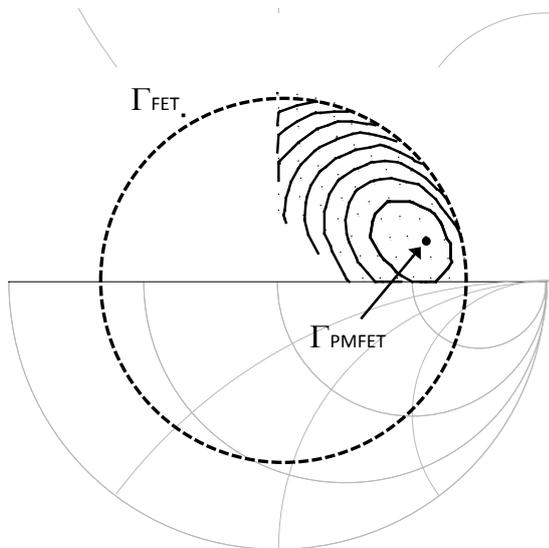
Fig. 2 Loadpull impedance of FET cell with pre-match circuit (Γ_{PMFET}) and its de-embedded impedance (Γ_{FET})
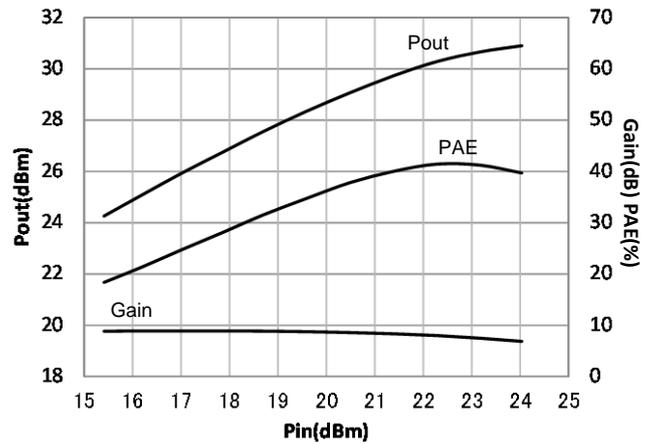
Fig. 3 Loadpull results of FET cell at 31GHz

IV. Circuit Design

Using the 50µm×8 FET cell as the basic cell, a 2-stage design was implemented to achieve a targeted gain of 13dB and an output power of 18W across 29GHz to 31GHz. Fig. 4 illustrates the block-diagram of the 2-stage MMIC. With a power-density of 3.3W/mm, the gate-width of the output amplifier stage was calculated as 6.4mm to meet the power specification. This corresponds to a 16 FET cells for an output power stage which was driven by an 8 FET cells for a driver stage (3.2mm). A staging ratio of 2:1 between the amplifier stages results in a good PAE versus bandwidth performance [14] while ensuring enough driving capability at the driver stage.
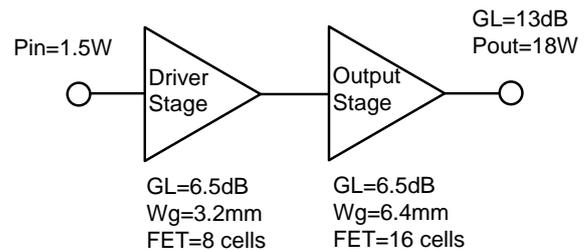
Fig.4 Block diagram of the 2-stage MMIC

The MMIC was designed to operate in Class-AB mode and reactively matched. Both the driver and the output power stage were matched to the measured loadpull impedance modeled by the RC equivalent circuit scaled to their required gate-width periphery. The matching networks were designed across a 12% bandwidth so as to meet the design goal with process variations. All the devices were made unconditionally stable by adding an RC-network in series with the gate, however, this reduced the linear gain of the MMIC by 2dB. Odd-mode oscillations were analyzed [15] and suitable resistors were added to both the gate and drain to avoid the oscillation. Stability was checked and ensured at the device, each individual amplifier stages and the full MMIC.

The circuits were simulated using Agilent's ADS and the coupling of the transmission lines at the matching networks was verified with extensive EM simulation. Fig. 5 shows the microphotograph of the fabricated GaN MMIC which measures 4.0mm×5.5mm.

V. MEASUREMENT RESULTS

For this initial evaluation step, the MMIC samples were measured on-wafer across 29GHz to 31GHz under pulsed drain bias of 10% duty cycle and 10μs pulse width to avoid thermal effects.

At VDD=24V, the MMIC achieved a saturated output power of 42.1dBm (16W) to 42.6dBm (18W) with an associated power gain of more than 5dB and drain efficiency of more than 13% across 29GHz to 31GHz.

For higher power requirement, the VDD was increased to 28V whereby the MMIC delivered a saturated output power of 42.8dBm (19W) to 43.3dBm (21W) with an associated power gain of more than 6dB and drain efficiency of more than 13% across 29GHz to 31GHz. The saturated output power peak at 30GHz with 21W, delivering an associated power gain of 6dB and drain efficiency of 16%. At VDD=28V, the MMIC had a linear gain of 10dB.

Fig. 6 shows the measured output power, efficiency and gain of the MMIC during saturation output power at VDD=24V and 28V. Fig. 7 and Fig. 8 show the measured power, efficiency and gain with swept input power at 29GHz, 30GHz and 31GHz when the MMIC was biased at VDD=24V and VDD=28V, respectively.
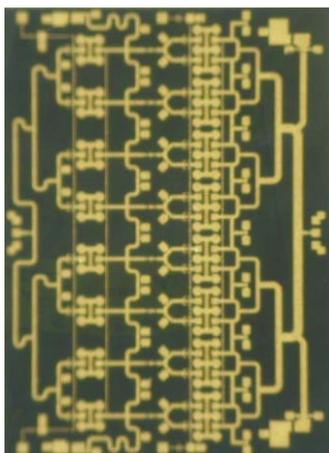
Fig. 5 Microphotograph of the developed GaN MMIC
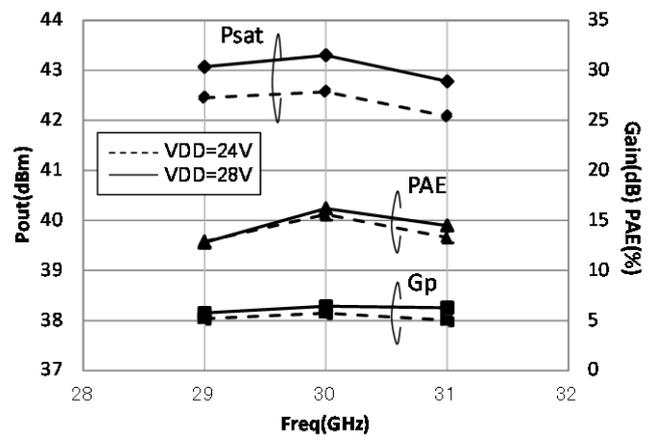
Fig. 6 Measured power, efficiency and gain at saturated output power
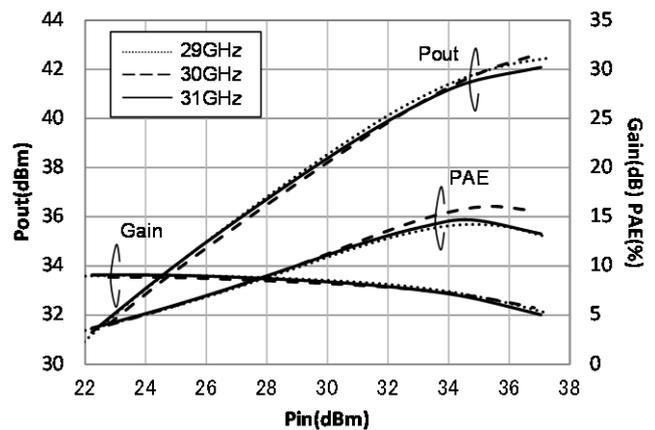
Fig. 7 Measured power, efficiency and gain with swept input power at VDD=24V
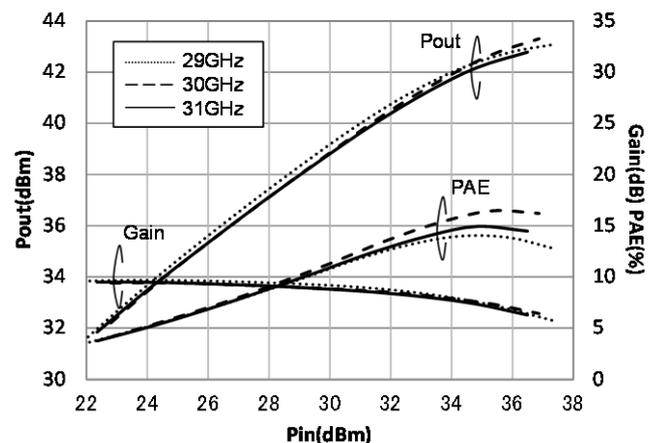
Fig. 8 Measured power, efficiency and gain with swept input power at VDD=28V

TABLE 1

Benchmarks of Ka-Band GaN HPA MMICs

Ref	Operating Condition	no. of stages	Freq (GHz)	Gain (dB)	Power (W)	PAE (%)	Area (mm^2)	Power/Area (W/mm^2)
[6]	CW	2	27	7	2.6	7	8.9	0.3
[7]	CW	2	28	13	4.0	24	—	—
[8]	CW	2	27	13	5.0	20	14.4	0.3
[9]	CW	2	35	12	4.0	23	—	—
[10]	CW	2	29	10	4.0	27	—	—
[11]	pulsed	3	29	25	5.0	30	4.8	1.0
[11]	pulsed	3	28.5	24	9.0	30	9.7	0.9
[12]	pulsed	3	29.5	28	5.8	32	5.6	1.0
[12]	pulsed	3	30	28	11.0	27	11.7	0.9
[13]	pulsed	2	30	23	7.9	28	17.3	0.5
This work	pulsed	2	30	10	21.4	16	22.0	1.0

Table1 benchmarks this work with the published Ka-band GaN high power amplifier MMIC of 2-stages or more. For MMICs that have results reported under both pulsed and CW operating conditions, the former was used for the comparison. It can be seen that the MMIC developed in this work achieved the highest output power performance which is nearly twice as much as the highest reported result. In terms of power per area, it is relatively high especially when compared to the other state-of-the-art MMICs of 2-stage configuration. However, the MMIC has low gain and efficiency. The linear gain of the MMIC was 3dB lower than expected and this was due to the mismatch loss incurred from process variations. The low gain degrades the efficiency of the MMIC by about 10% from the targeted value.

VI. CONCLUSION

A high-power MMIC developed from in-house 0.18μm gate-length GaN HEMT process is demonstrated at Ka-band. Under pulsed bias condition at VDD=28V, the MMIC achieved a saturated output power of 19W to 21W across 29GHz to 31GHz. This is believed to be the highest ever reported Ka-band GaN MMIC and this MMIC can be expected to further enhance Ka-band SATCOM systems' performance in terms of higher output power and smaller size.

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