

Effects of Via Layout on AlGaIn/GaN HEMTs at Ka-band

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Keywords: ...GaN, AlGaIn, HEMT, Ka-band

Abstract

We report on the effects of via layout design for high frequency device. This study experimentally showed that the source inductance of the device influences its f_{max} characteristic. Increasing the number of vias and through innovative layout patterns, the maximum frequency of the device can be increased. Using a novel layout pattern, an 8-cells discrete power device (total gate-width=3.2mm) has been demonstrated at Ka-band.

INTRODUCTION

A promising candidate for the next generation of microwave power devices, AlGaIn/GaN HEMT has aroused numerous research interests due to its inherent high power characteristic. It has been studied intensively as high power microwave devices for satellite communication systems and in recent years, many GaN-based HEMTs have been reported for power amplification applications at Ka-band [1-3].

High gain is a desirable characteristic for a microwave device as the gain affects its efficiency and consumption power. One of the methods to achieve high gain at ka-band for HEMT device is to increase its f_{max} by shortening the gate-length to less than $0.2\mu\text{m}$. However, fabricating short gate-length GaN HEMT is difficult due to the increasing leakage current and lower breakdown voltage. A simpler method to achieve high gain performance is to reduce the source inductance of the device. This inductance is contributed mainly by the physical layout of the vias at the source terminal and is independent on the device's leakage current or breakdown voltage. In this paper, we report on the effects of via, in particularly its layout on the performance of the GaN HEMT device.

EXPERIMENT

GaN HEMT device with gate-length of $0.2\mu\text{m}$ is fabricated on 3-inch SiC substrate. The HEMT structure is based on $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ epitaxial layers grown by MOCVD. Via-holes are formed by ICP-RIE and the back-

side of the wafer is thinned to $50\mu\text{m}$ by mechanical polishing. In this study, $50\mu\text{m}$ unit gate-width GaN HEMT devices with various layouts of via patterns are fabricated and their small-signal gain characteristics are then compared using Vector Network Analyzer. The setting bias is $V_{ds}=24\text{V}$ and $I_{ds}=1/3I_{dss}$. For power evaluation, loadpull measurements were performed at 31GHz.

RESULTS AND DISCUSSION

GaN HEMT devices of 2, 8, 12 gate-fingers with side-vias layout as shown in figure 1 are compared. The difference in number of gate fingers resulted in different source terminal interconnections, and therefore different source inductances. Figure 2 shows the measured small-signal gain characteristics. At frequency higher than 30GHz, Type A (2 gate-fingers) achieved the highest gain due to a smaller source inductance which affects the maximum frequency at which MSG is maintained.

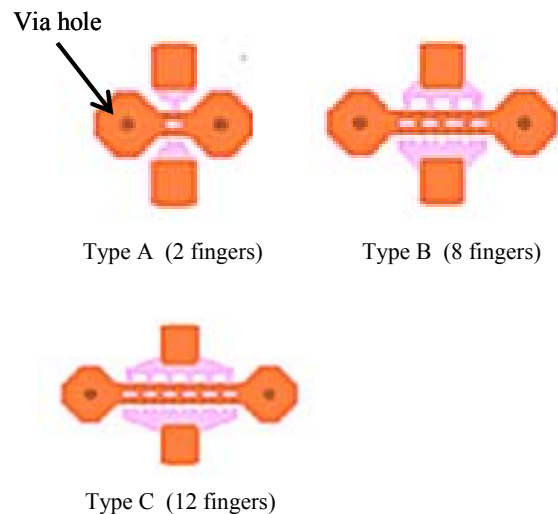


Figure 1 Device layout of 2, 8, 12 gate-fingers with side-vias. All unit gate width is $50\mu\text{m}$.

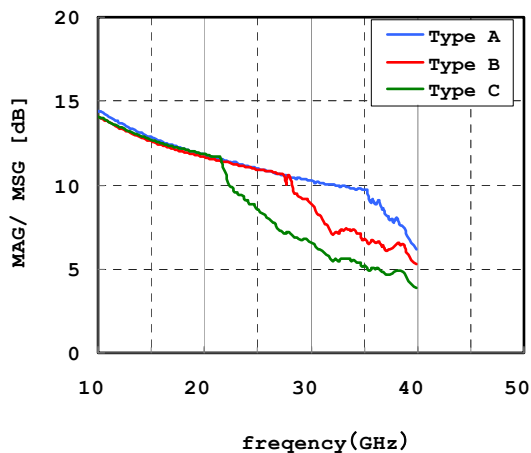


Figure 2 Small signal gain characteristics of Type A, B, C.

However, for high-power applications, Type A device needs to be paralleled, and the total number of vias increases the size of the device significantly.

Fixed gate width of $400\mu\text{m}$ ($50\mu\text{m} \times 8$) devices with various via layout patterns as shown in figure 3 are next compared. Figure 4 shows the measured small-signal gain characteristics of these devices. Comparing with reference Type B (side-vias), Type D which has the vias near to the gate-pad achieved lower gain above 30GHz.

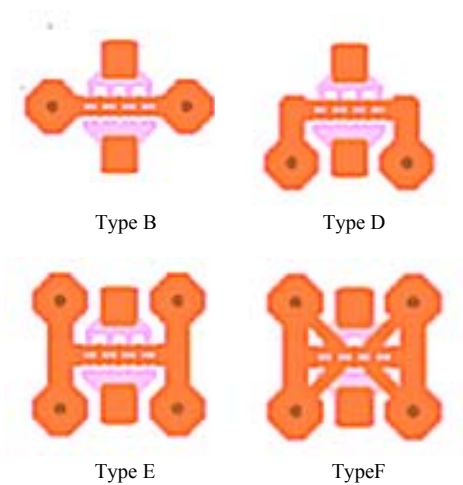


Figure 3 Various via layout patterns. Each device has 8 gate fingers.

This can be explained by the physical layout connection extending from the source terminal to the vias, which increases the source inductance. To reduce this effect, Type E with the number of vias increased, and Type F an

innovative layout using air-bridge to shorten the connection have both been designed. These two types of patterns increased the maximum frequency of the achievable MSG as compared to Type B. Moreover, both patterns can shrink the size of the layout, an advantage for implementing compact high power devices.

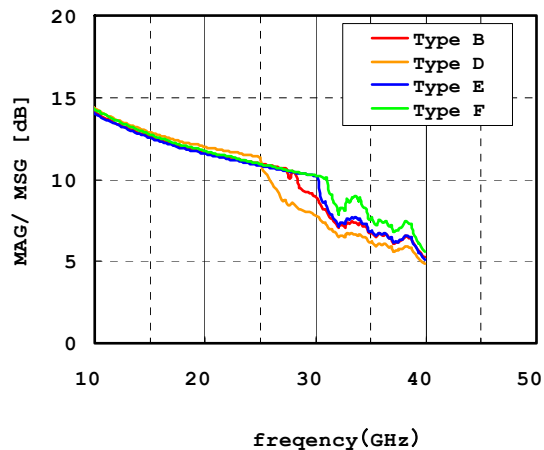


Figure 4 Small signal gain characteristics of Type B, D, E, F.

A loadpull measurement at 31GHz is performed on Type E (4 via-holes) device biased at 24V. A saturation output power of 32.6dBm (4.5W/mm), linear gain of 7.3dB and PAE of 41% have been achieved as shown in Figure 5.

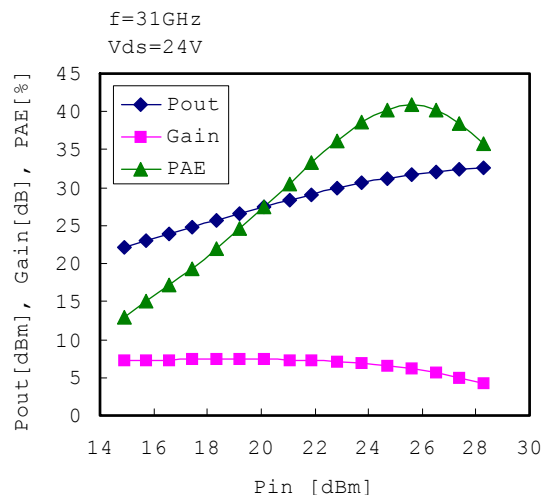


Figure 5 Loadpull measurement of Type E device at frequency= 31GHz and $V_{ds}=24V$.

With Type F layout pattern, an 8-cells discrete power device (total gate-width=3.2mm) as shown in figure 6 has been designed at Ka-band. The power device biased at 24V is matched to 31GHz with input and output matching circuits. Measured on a carrier-plate, the device has an output power reaching 9.2W (39.6dBm), a linear gain of 6.3dB and maximum PAE of 22.8%.

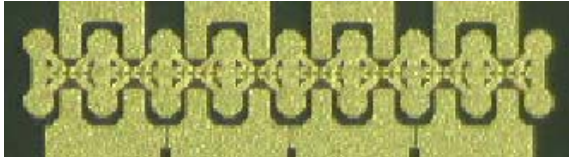


Figure 6 Power device of 3.2mm gate width at Ka-band.

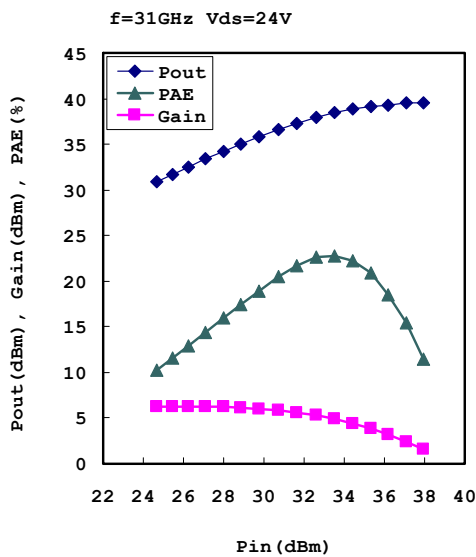


Figure 7 Input-output characteristics of a 8-cell HEMT on a metal carrier plate at 31GHz and Vds is 24V.

CONCLUSIONS

We have designed GaN HEMT devices with various via layout patterns and have experimentally shown that the source inductance influences the gain of the device by comparing their f_{max} . With a novel layout pattern, an 8-cells discrete power device is demonstrated at 31GHz. Biased at 24V, the discrete power device achieved an output power of

9.2W (39.6dBm), a linear gain of 6.3dB and a maximum PAE of 22.8%.

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ACRONYMS

f_{max} : maximum frequency of oscillation