TOSHIBA

DOCUMENT No. 803-180014

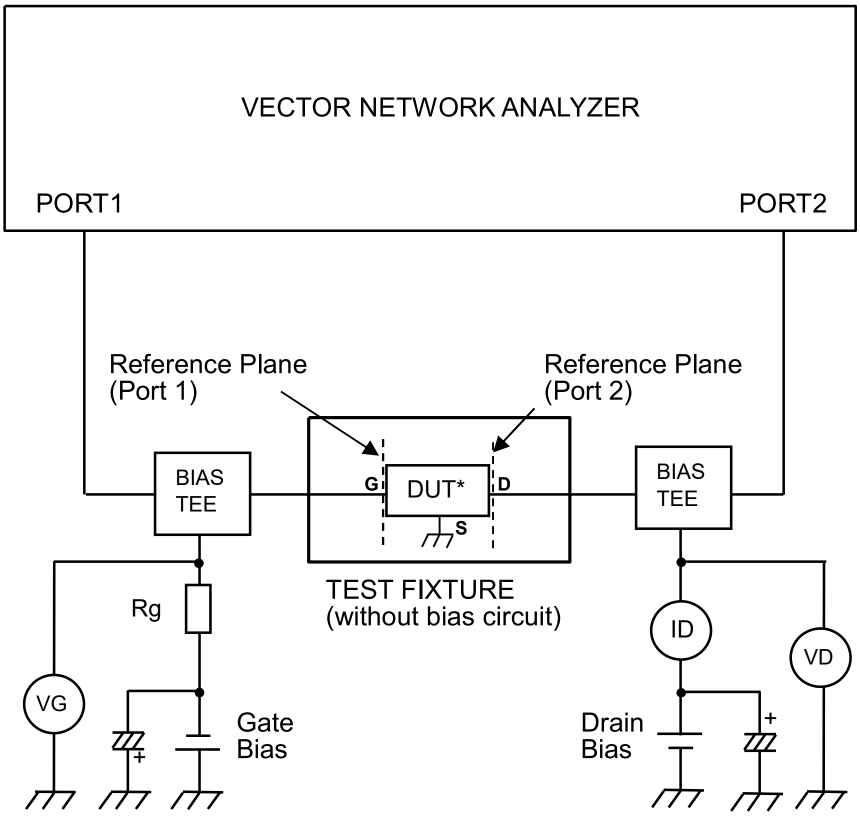
MICROWAVE SEMICONDUCTORS

ELECTRICAL MEASUREMENT

CONTENTS

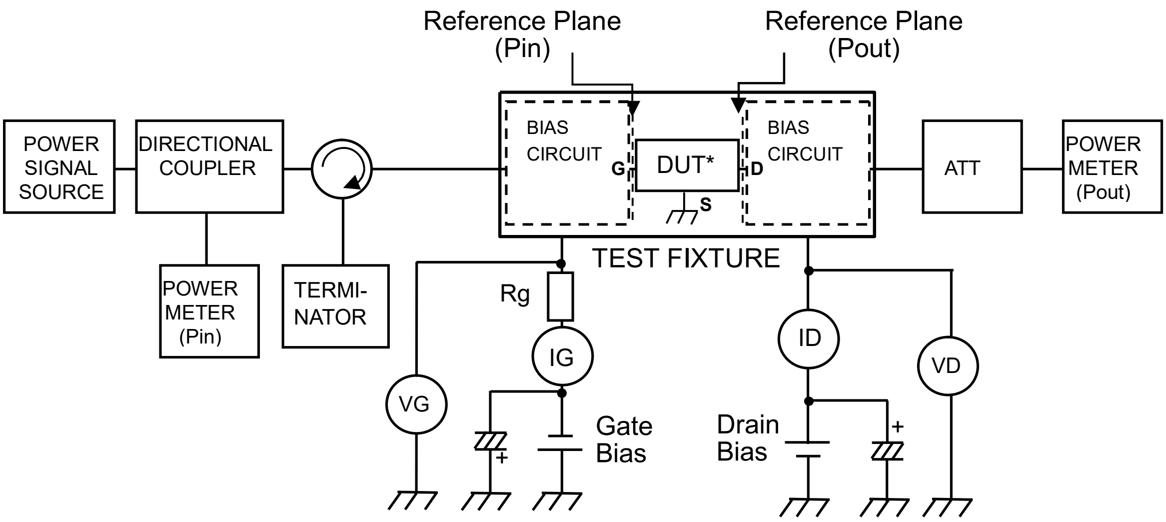
TOSHIBA

A. S-PARAMETER MEASUREMENT SYSTEM BLOCK DIAGRAM



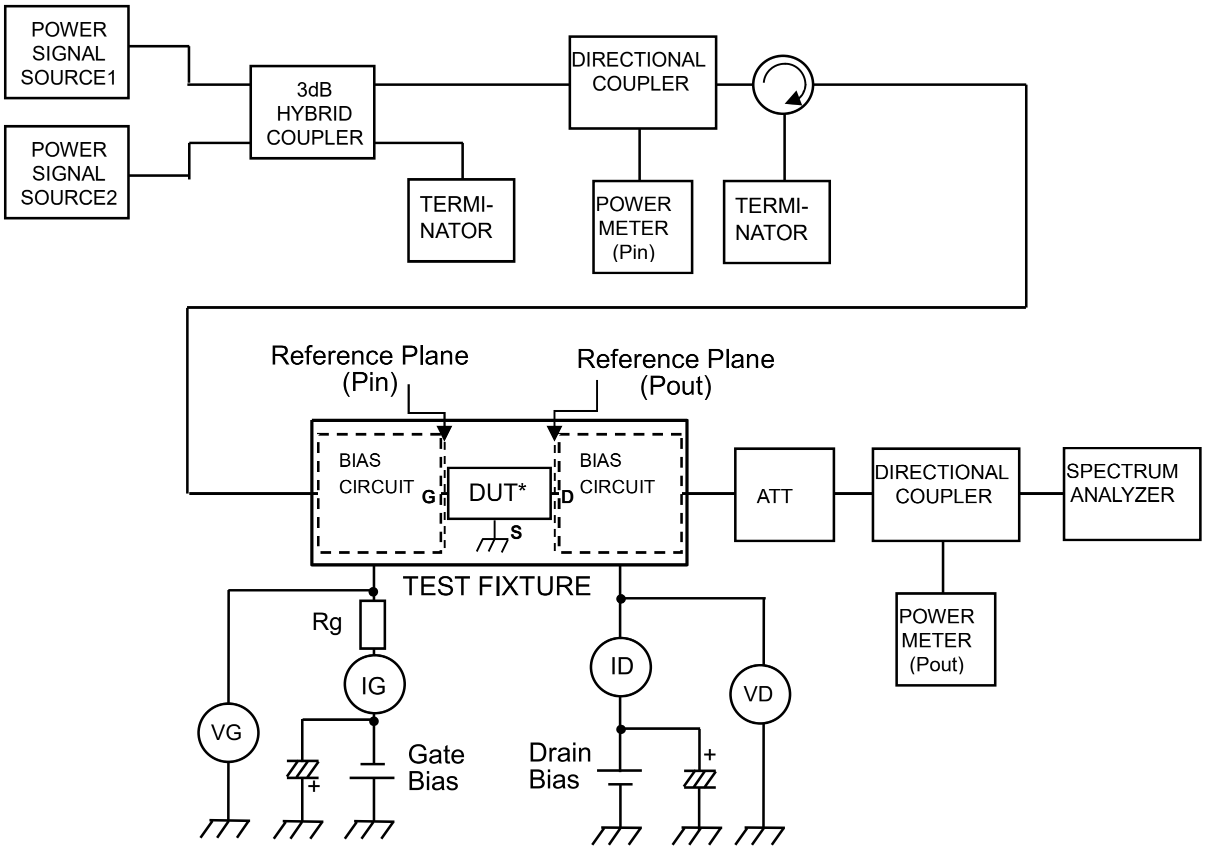
*DUT: Device Under Test

B. POWER TEST SYSTEM BLOCK DIAGRAM



*DUT: Device Under Test

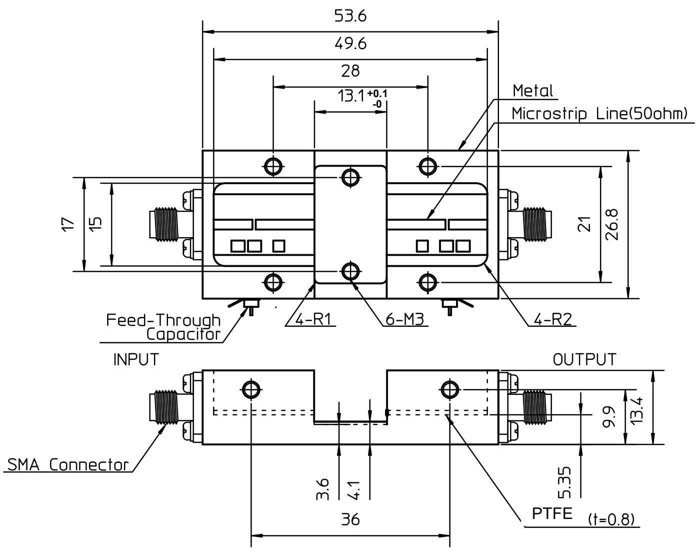
C. IM3 & POWER TEST SYSTEM BLOCK DIAGRAM



*DUT: Device Under Test

D. TESTFIXTURE

(1) TESTFIXTURE (C-band medium package)



C-BAND

(GaAs 4W, 6W, 8W)

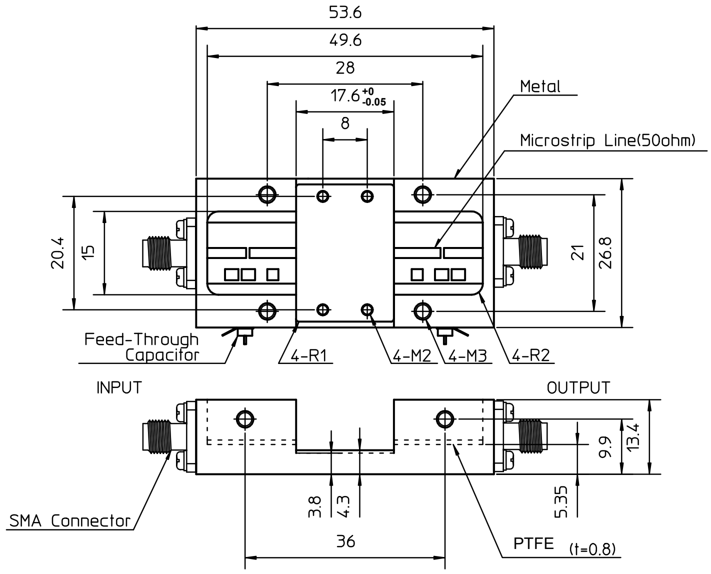
(GaN 50W, 60W)

PACKAGE CODE:

2-11D1B

7-AA04A

(2) TESTFIXTURE (C-band large package)



C-BAND

(GaAs 12W, 16W, 25W,

30W, 35W, 45W, 60W)

(GaN 120W, 130W)

PACKAGE CODE:

2-16G1B

7-AA05A

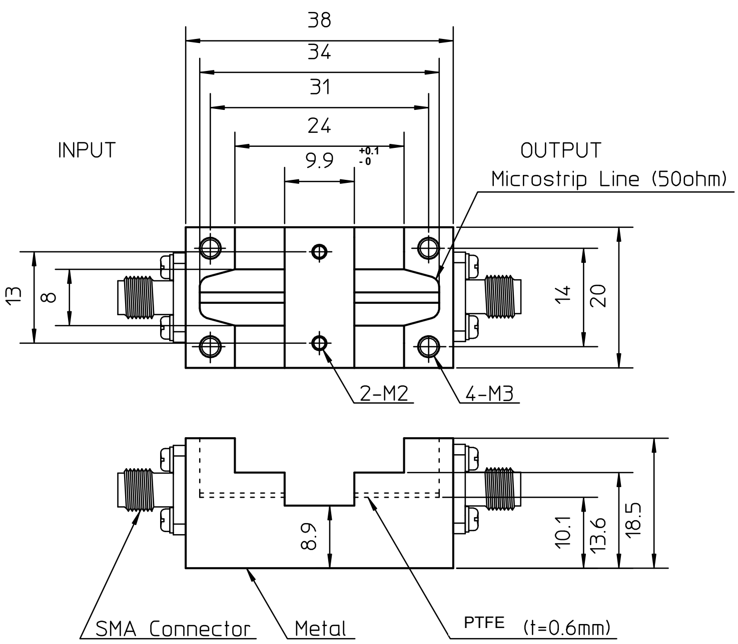
7-AA09A

7-AA06A

(Unit in mm)

Note: An appropriate metal block (for example, made of alminum) should be used with the test jig to get a good heat flow.

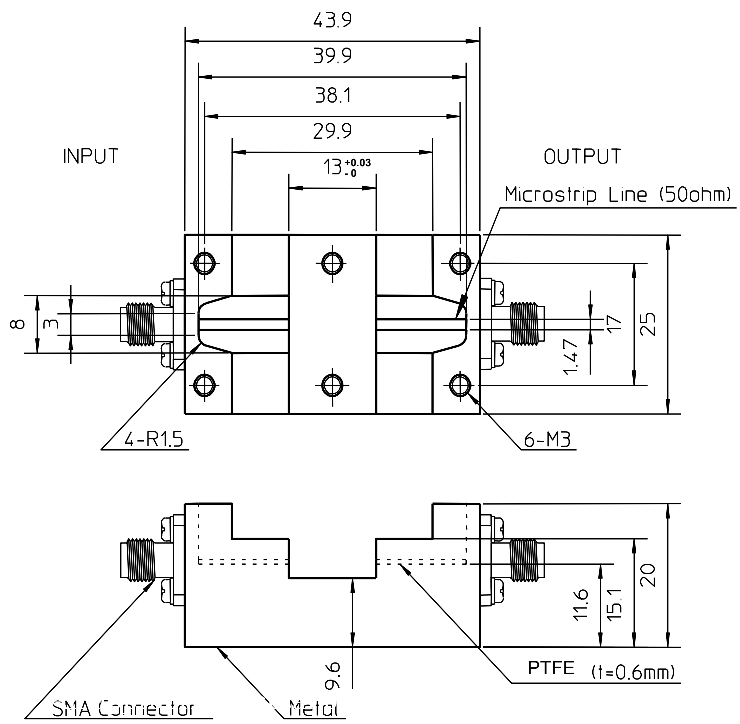
(3) TESTFIXTURE (X/Ku-BAND small package)



X/Ku-Band
(GaAs 2W, 4W, 5W, 7W, 8W, 9W)

PACKAGE CODE:
2-9D1B

(4) TESTFIXTURE (X/Ku-BAND medium package)



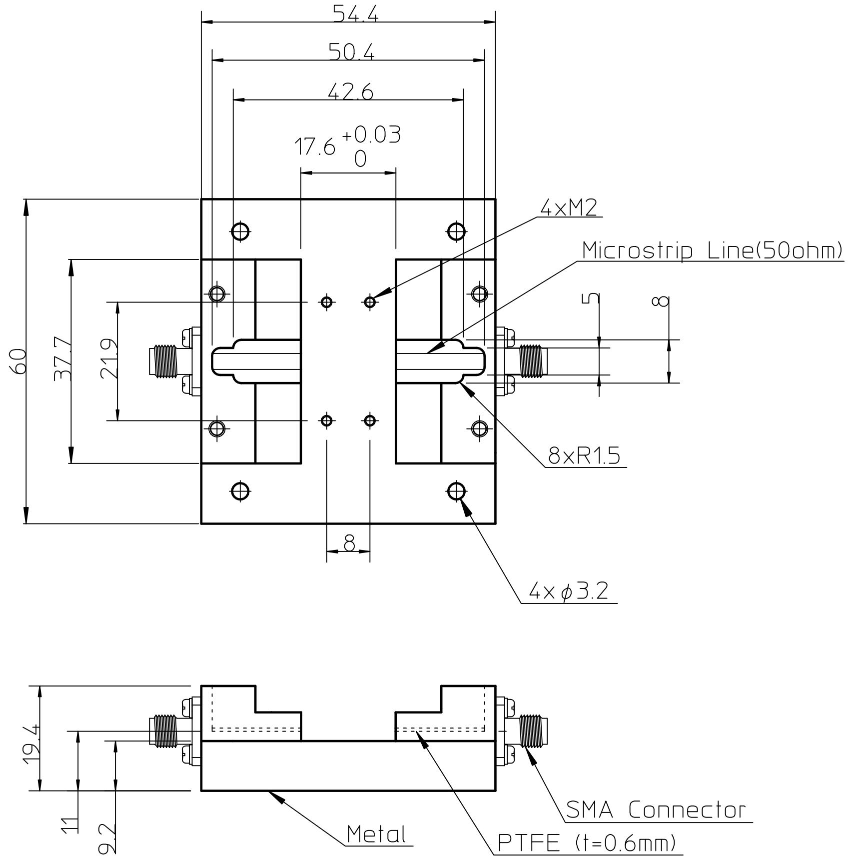
X/Ku-Band
(GaAs 8W, 10W, 15W, 18W)
(GaN 25W, 50W)

PACKAGE CODE:
2-11C1B
7-AA04A
7-AA07A

(Unit in mm)

Note: An appropriate metal block (for example, made of alminum) should be used with the test jig to get a good heat flow.

(5) TESTFIXTURE (X/Ku-BAND large package)



X/Ku-Band

(GaAs 30W)

PACKAGE CODE:

7-AA03B

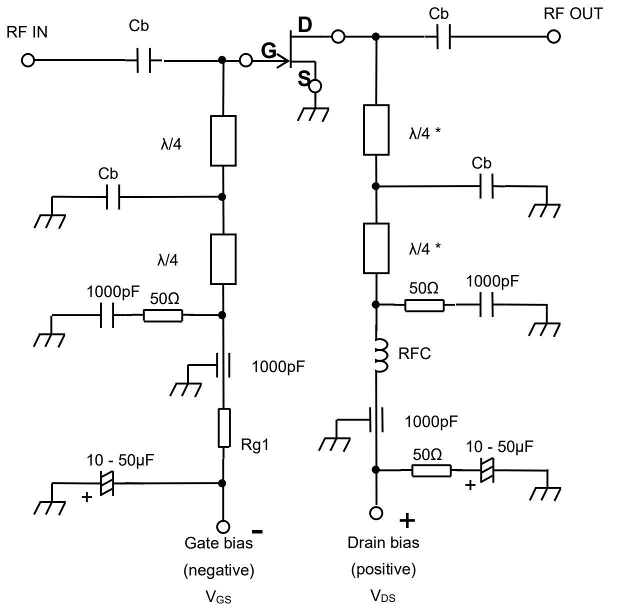
(Unit in mm)

Note: An appropriate metal block (for example, made of alminum) should be used with the test jig to get a good heat flow.

E. RECOMENDED BIAS CIRCUIT

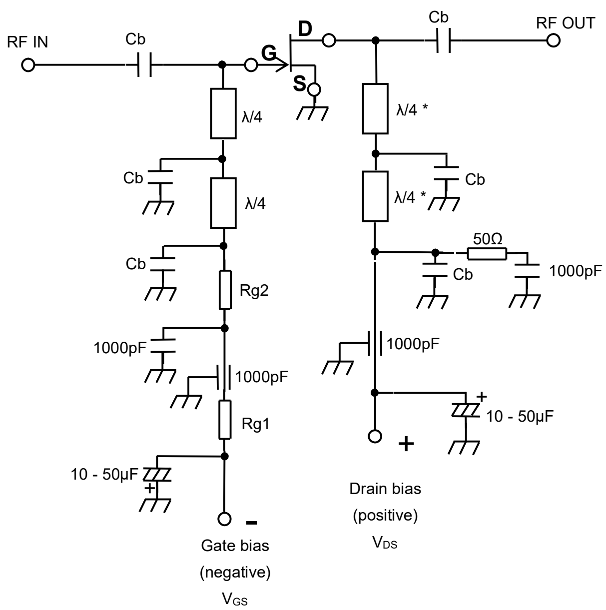
Recommended bias circuits are as follows.

(1) BIAS CIRCUIT for L/S-BAND



PRODUCT	Cb(pF)	Rg1(Ω)
GaAs 60W	10 to 15	30

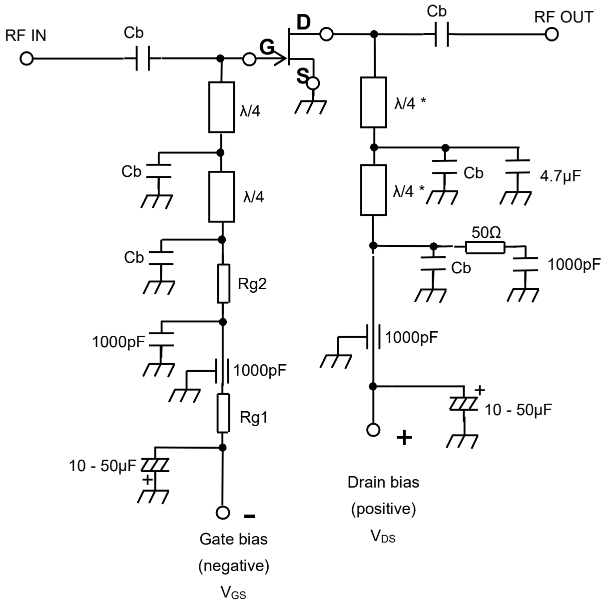
(2) BIAS CIRCUIT for C-BAND (GaAs 4 to 60W, GaN 25 to 50W)



PRODUCT		Cb(pF)	Rg1(Ω)	Rg2(Ω)
C-BAND GaAs	4W, 6W, 8W	1 to 3	100	50
	12W, 15W, 16W		50	18
	25W, 30W, 35W, 45W, 60W		10	18
C-band GaN	25W, 50W		10	50

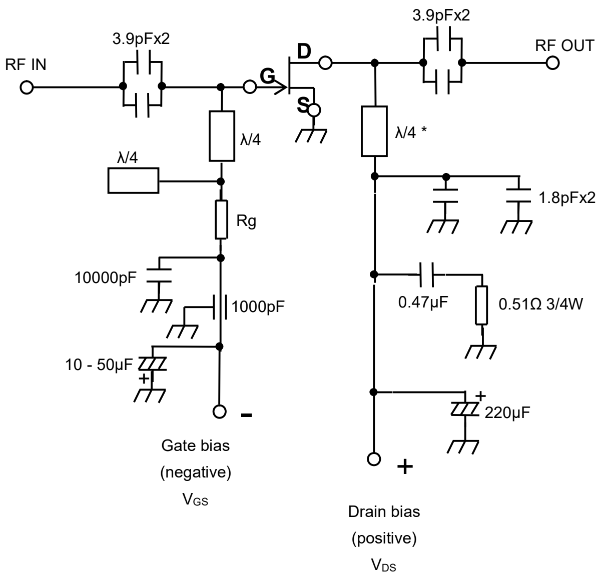
CAUTION: To avoid fusing the trace on PCB, the cross section of drain biasing line(*) should be made large enough.

(3) BIAS CIRCUIT for C-BAND (GaN 120W)



PRODUCT		Cb(pF)	Rg1(Ω)	Rg2(Ω)
C-BAND GaN	120W	1 to 3	10	18

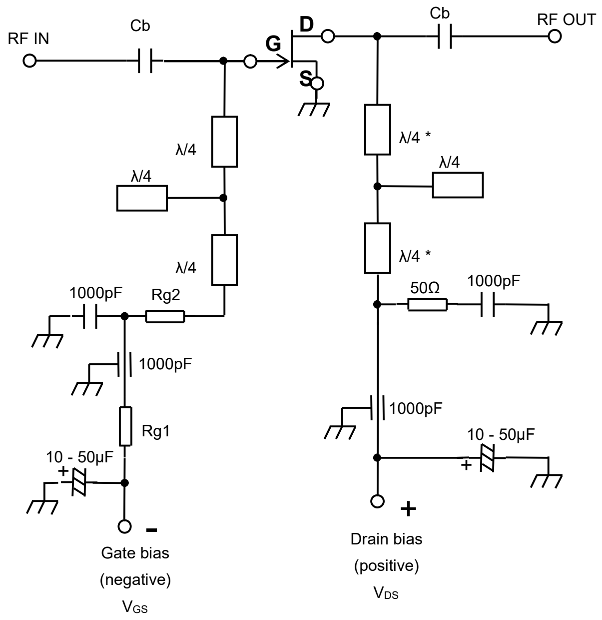
(4) BIAS CIRCUIT for C-BAND (GaN 60W, 130W)



PRODUCT		Rg(Ω)
C-BAND GaN	60W, 130W	10

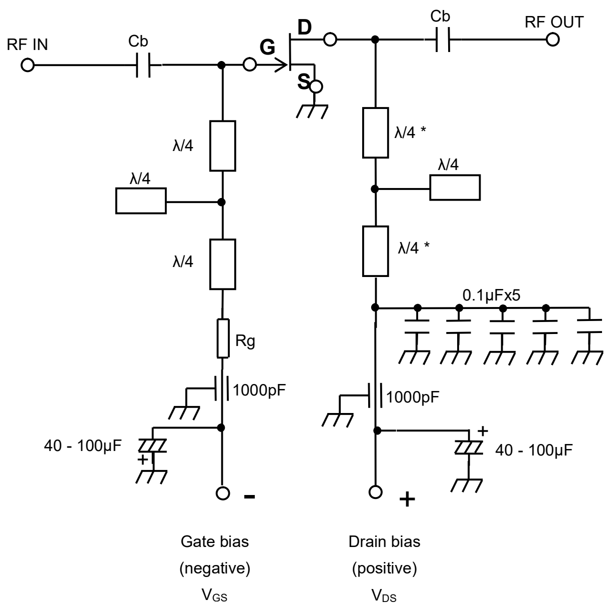
CAUTION: To avoid fusing the trace on PCB, the cross section of drain biasing line(*) should be made large enough.

(5) BIAS CIRCUIT for X/Ku-BAND (GaAs 2 to 18W)



PRODUCT		Cb(pF)	Rg1(Ω)	Rg2(Ω)
X/Ku-BAND GaAs	2W, 4W, 5W, 7W, 8W, 9W	0.5 to 1	100	50
	10W, 15W, 18W		50	50

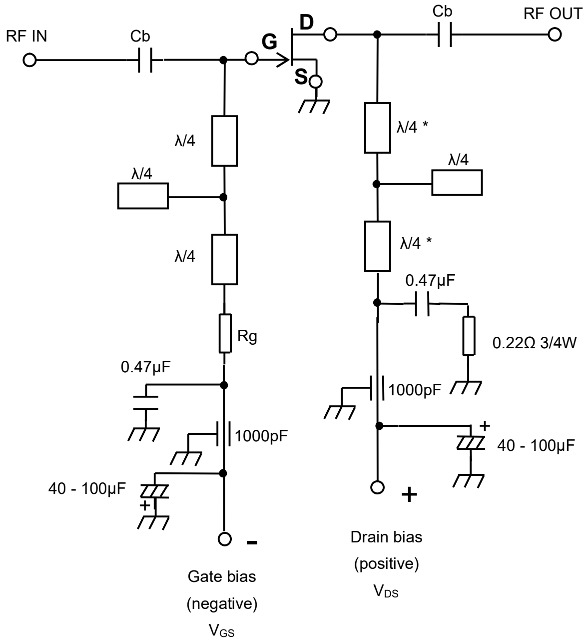
(6) BIAS CIRCUIT for X/Ku-BAND (GaAs 30W)



PRODUCT		Cb(pF)	Rg(Ω)
X/Ku-band GaAs	30W	0.5 to 2	10

CAUTION: To avoid fusing the trace on PCB, the cross section of drain biasing line(*) should be made large enough.

(7) BIAS CIRCUIT for X/Ku-BAND (GaN 25W, 50W)



PRODUCT		Cb(pF)	Rg(Ω)
X/Ku-band GaN	25W, 50W	0.5 to 2	13.3

CAUTION: To avoid fusing the trace on PCB, the cross section of drain biasing line(*) should be made large enough.

F. METHOD FOR THERMAL RESISTANCE MEASUREMENT

The thermal resistance of GaAs FETs can be measured by using drain to source voltage (V_{DS}) pulse to produce various voltages across the forward-biased gate to source junction, as shown in Figure A. The constant gate forward current (I_M) is chosen small enough not to cause the device heating excessively nor burn-out but of sufficient magnitude to ensure reliable reading of V_{GSF}.

When heating power (I_{DS} X V_{DS}) is applied to the FET during the period "T," the channel temperature increases and V_{GSF} decreases, due to the temperature characteristics of V_{GSF} shown in Figure B. After a sufficient time to ensure that the channel temperature has stabilized at its new value, V_{DS} is quickly reduced to zero. If V_{GSF1} and V_{GSF2} are the value of V_{GSF} before and after heating, the difference $\Delta V_{GSF} = V_{GSF1} - V_{GSF2}$ is related to the channel temperature increase (ΔT_{ch}) as follows;

$$\Delta V_{GSF} = \Delta T_{ch} / K$$

Note: K is the temperature coefficient for ΔV_{GSF} under constant I_M.
Using ΔT_{ch} determined by above equation, the thermal resistance $R_{ch(c-c)}$ between channel and flange of the FET is obtained as follows;

$$R_{ch(c-c)} = \Delta T_{ch} / (I_{DS} \times V_{DS}) = (K \times \Delta V_{GSF}) / (I_{DS} \times V_{DS}) \quad (°C / W)$$

The thermal resistance value obtained by the above electrical measurement is calibrated by IR (Infra-Red) measurement results because IR measurement has better resolution than the above measurement technique.

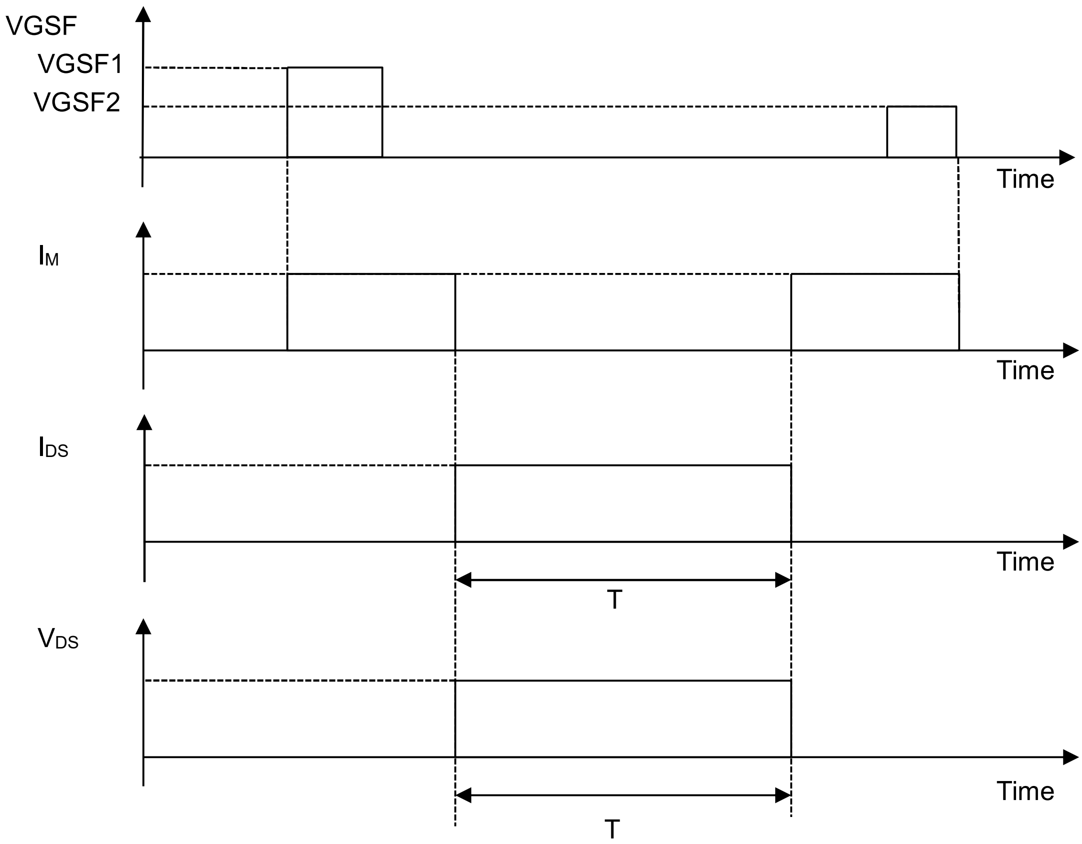


Figure A Timing Diagram

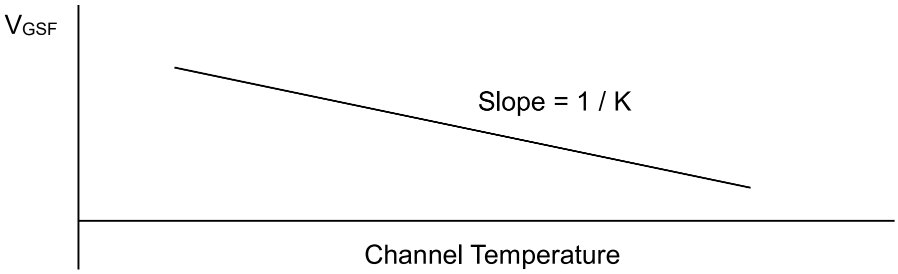


Figure B Forward Biased Gate to Source Voltage vs. Channel Temperature