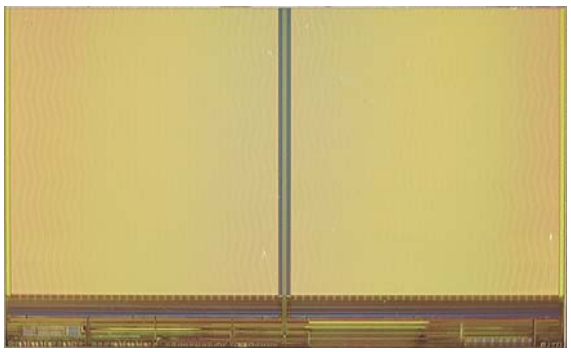
64 Gbit Large-Capacity MLC (4-Level Cell) NAND Flash Memory Using 24 nm Process Technology



World's smallest 64 Gbit MLC (4-level cell) NAND flash memory chip

NAND flash memories have a variety of applications such as mobile phones, music players, smartphones, solid-state drives (SSDs), and memory cards, taking advantage of its features of large capacity and low bit cost. It has therefore become an indispensable device in daily life.

With San Disk Corporation in the United States, Toshiba has jointly developed the world's smallest(*) 64 Gbit multilevel cell (MLC: 4-level cell) NAND flash memory using 24 nm process technology to meet the strong market demand for further expansion of capacity and bit-cost saving.

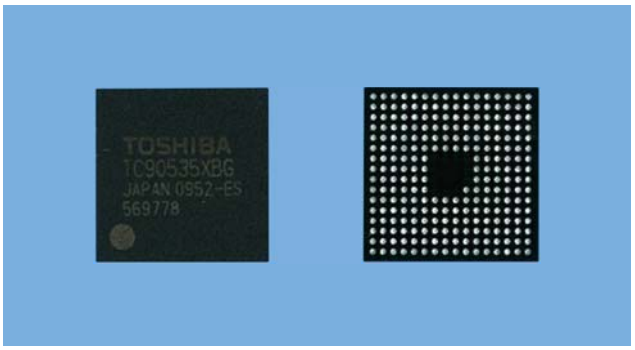
Changes in the readout architecture from the memory cells and an innovative circuit design have realized a substantial reduction of the peripheral circuit area, which is the area other than the memory cell array, resulting in a reduction of chip area by 40% compared with equivalent-capacity products using the 32 nm process in the previous generation.

The built-in toggle double data rate (DDR) interface achieves a data transfer speed three times faster than conventional interfaces to provide the high-speed data transfer required by SSDs and data servers.

In addition, a new circuit technology overcomes degradation of the device characteristics through technology scaling, and realizes the same high-speed writing performance as the previous generation.

(*) As of August 2010 (as researched by Toshiba)

TC90535XBG Low-Power-Consumption Baseband LSI for Wireless LAN



TC90535XBG wireless LAN baseband LSI achieving low power consumption

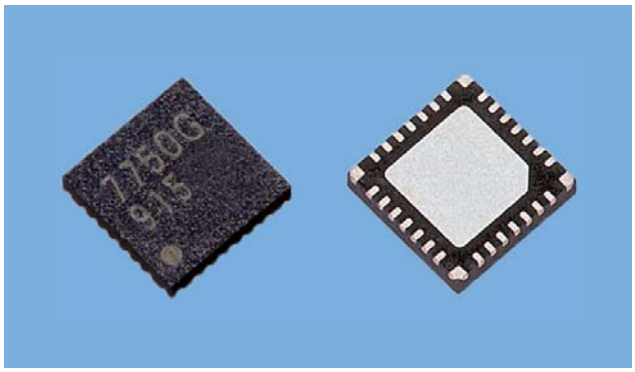
The application of wireless LAN has expanded from PCs to mobile devices and is further penetrating into home appliances, requiring large-scale integrations (LSIs) for wireless LAN with low power, low cost, and high throughput.

To meet this requirement, Toshiba has developed a baseband LSI compliant with the latest wireless LAN standard, IEEE 802.11n, achieving a high throughput of 72 Mbits/s and one of the lowest levels of power consumption for such devices in the world.

To achieve this low power consumption, the circuit blocks are divided into multiple power domains to dynamically control the power supply voltage. Technologies for clock frequency control and original low-power flip-flops are also employed. In addition, the embedded 32-bit reduced instruction set computer (RISC) processor core is capable of handling tasks up to the level of communication middleware and applications in order to reduce the load of the host processor.

IEEE: Institute of Electrical and Electronics Engineers

TC7750FTG DC-DC Converter IC Realizing Industry's Smallest Single-Channel Digital Control System



TC7750FTG digitally controlled DC-DC converter IC

As the first step of a digitally controlled regulator, Toshiba has developed a monolithic 3A-class digital DC-DC converter integrated circuit (IC) for a single-channel noninsulated digital feedback system.

Digitization of the existing analog system allows self-control of the device voltage, current, and temperature as well as the PID control function(*1) that promptly responds to load variations. In addition, the PMBus communication interface for power supply control enables communication with a microcomputer and on-board control of system conditions.

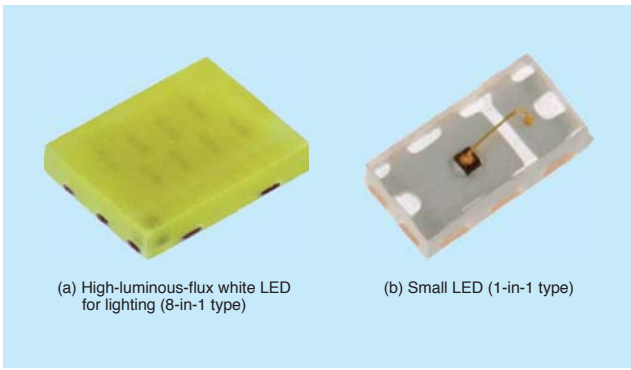
Furthermore, we have realized the industry's smallest size(*2) with the small QFN28 package.

For the future, we will expand the product lineup to correspond to high current using the digital feedback system.

(*1) PID is a type of feedback control that combines the three elements of P (proportional), I (integral), and D (derivative).

(*2) As of September 2010 among digitally controlled DC-DC converter ICs (as researched by Toshiba)

See-Through Type LED Using New Surface-Mounting Package



LEDs in see-through packages

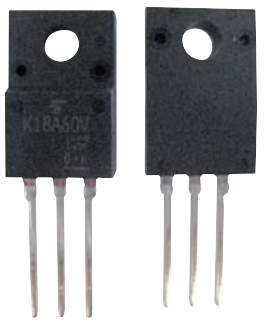
Toshiba has developed a see-through type light-emitting diode (LED) as a new package surface-mounting product.

In the manufacturing of surface-mounting LEDs, a different molding resin die is generally used for each product. For newly developed LED, on the other hand, a lead frame is totally encapsulated with resin by compression molding, and the lead frame and mold resin are separated at one time by dicing to manufacture the product.

Consequently, the same assembly lines can be used to manufacture various types of LEDs with package sizes ranging from small (1.6 mm × 0.8 mm) to large (3.1 mm × 3.8 mm) simply by changing the layout design of the lead frame, leading to a marked improvement in cost performance.

We are promoting the development of various types of products in this category, including high-luminous-flux white LEDs for lighting (8-in-1 type), small LEDs (1-in-1 type) for use as indicators in various equipment, and tri-color (red, green, and blue) LEDs (3-in-1 type).

MOSFET DTMOS Series with Third-Generation Super-Junction Structure



DTMOS series third-generation MOSFETs with super-junction structure (TK18A60V)

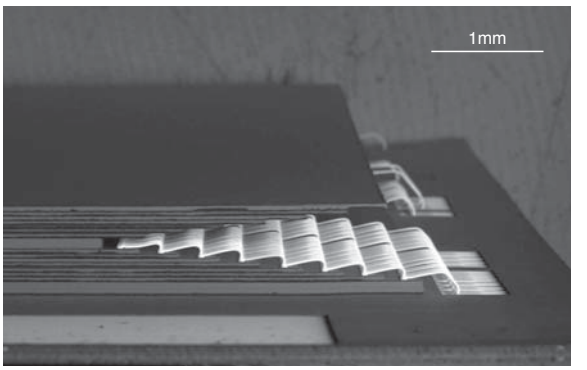
Toshiba has developed the DTMOS III as the third generation of the DTMOS series based on a super-junction structure in the field of high-voltage power metal-oxide-semiconductor field-effect transistors (MOSFETs) applied to switching power supplies for electronic devices, inverters for solar-power generation systems, DC/DC converters for hybrid vehicles, etc.

There is strong market demand for high efficiency and downsizing in the application of switching power supplies and inverters, and high-voltage power MOSFETs are required to achieve loss minimization and size reduction by decreasing the on-resistance. We have employed the super-junction structure, which realizes the miniaturization of MOSFETs and low on-resistance surpassing silicon (Si) boundaries, to commercialize a low-on-resistance product. The super-junction structure is designed to periodically allocate the p-layer and n-layer in the drift layer (n-layer) in the direction perpendicular to the chip.

Our MOSFET DTMOS II, as the second-generation product with a super-junction structure, realized high-speed switching characteristics through a low-capacity design without any change in the noise characteristics. The new DTMOS III, as the third-generation product, features low on-resistance as well as an optimized gate structure, leading to improvement of the noise characteristics. Consequently, the on-resistance is reduced by approximately 12% compared with the DTMOS II (of the same chip size), and the rate of voltage change (dv/dt) is restrained by approximately 30% at the turn-off that may generate noise (under the condition of identical gate resistance).

We are further expanding our product lineup to encompass high-voltage products and high-speed products with built-in diodes on the basis of this design technology.

128 Gbyte *e*•MMC™ Embedded NAND Flash Memory with Industry's Largest Capacity



Internal structure of 128 Gbyte *e*•MMC™ embedded NAND flash memory

The *e*•MMC™ is a memory device whose interface is compliant with the JEDEC (Joint Electron Device Engineering Council) *e*•MMC standard Ver. 4.4, consisting of 16 stacked 64 Gbit NAND chips fabricated using the 32 nm process and a controller chip in a JEDEC small package.

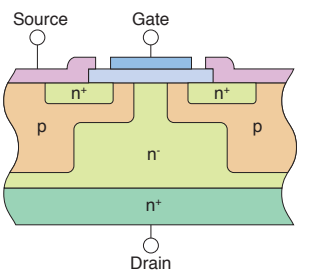
Toshiba has commercialized the 128 Gbyte *e*•MMC™ with the largest capacity(*) in the industry by accomplishing 17-layer stacking of chips (a 16-layer stack of NAND chips and a controller chip) based on cutting-edge technologies including 30 µm-thickness chip technology and chip-stacking technology.

The *e*•MMC™ allows easy embedding in mobile devices and reduction of the user's development load.

A lineup of seven types of *e*•MMC™ from 128 Gbytes to 2 Gbytes is available to meet the needs of mobile devices such as smartphones and tablet PCs.

(*) As of April 2011 among embedded NAND flash memories (as researched by Toshiba)

e•MMC is a trademark of JEDEC.



Structure of super junction

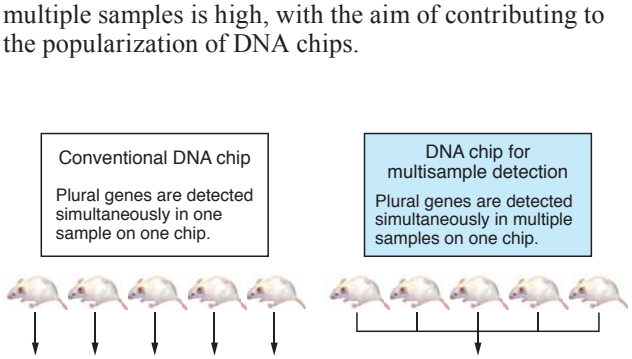
Development of DNA Chip for Multiple Samples

Toshiba has developed a novel DNA (Deoxyribonucleic acid) chip technology for multiple samples in order to improve the cost performance of DNA chips. The new DNA chip can detect plural genes in multiple samples, whereas the conventional DNA chip can only detect plural genes in a single sample.

The new technology, realized by a new sample identification technique using tag sequences, has the following advantages:

- The cost per sample is drastically reduced through the detection of multiple samples by one DNA chip.
- Operation is simple and the new DNA detection system is compatible with the conventional system.
- Accuracy is high and there is no false positive detection.

The new technology was first applied to a DNA chip for monitoring microbiological diseases in experimental animals, which was launched as the "MoniGene™ Helico-Multi" in June 2010. We plan to expand the application of DNA chips using this new technology to the infectious disease diagnosis field where demand for the testing of multiple samples is high, with the aim of contributing to the popularization of DNA chips.



DNA chip for multisample detection

Silicon Nitride Substrates with High Thermal Conductivity for EVs and HEVs

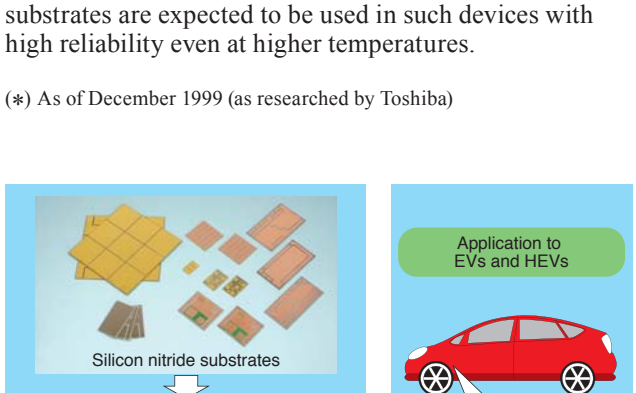
The application of silicon nitride (Si_3N_4) substrates with a high thermal conductivity of 90 W/(m•K) for the power control unit (PCU) of electric vehicles (EVs) and hybrid electric vehicles (HEVs) has been increasing. Si_3N_4 possesses excellent mechanical properties such as bending strength, fracture toughness, and hardness.

Toshiba Materials Co., Ltd. has developed an Si_3N_4 substrate with high thermal conductivity while maintaining its mechanical properties for the first time(*) in the world by optimizing the powders, sintering aids, and sintering conditions used in its manufacture.

The main properties of the newly developed substrate are a thermal conductivity of 80 to 90 W/(m•K) a bending strength of 650 MPa, and a fracture toughness of 6 to 7 $MPa•m^{1/2}$. A thin Si_3N_4 substrate of 0.32 mm in thickness with a thick copper pattern of about 0.6 mm in thickness was developed to provide the lower thermal resistance required for higher output per volume of the PCU, and showed no cracks after being subjected to a thermal cycle test of 3 000 cycles. Furthermore, it is possible to increase the productivity of the PCU by employing Si_3N_4 substrates in which ultrasonic welding can be used between the copper patterns and terminals, or rivets can be used for direct jointing to the base plate.

Devices made of silicon carbide and gallium nitride as the next-generation power semiconductors will have a high junction temperature exceeding 200°C. Si_3N_4 substrates are expected to be used in such devices with high reliability even at higher temperatures.

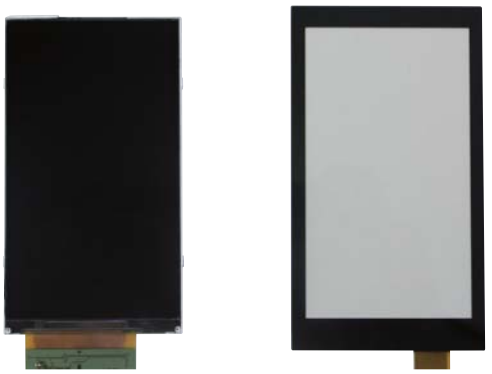
(*) As of December 1999 (as researched by Toshiba)



IGBT: insulated-gate bipolar transistor

Silicon nitride substrates with high thermal conductivity

Development of LCD Module with Capacitive Touch Panel for Smartphones



4-inch full wide video graphics array (FWVGA: 854 × 480 pixels) LCD module (left) and capacitive touch panel module (right)

Toshiba Mobile Display Co., Ltd. has developed a large, high-resolution liquid crystal display (LCD) and a capacitive touch panel for use in smartphones.

The capacitive touch panel, composed of the glued combination of a thin capacitive touch sensor glass of 0.5 mm in thickness and a tempered-cover glass using ultraviolet (UV)-cured adhesive, detects an electrical charge moving from the panel surface when a finger touches it. The design has been totally optimized to match the visibility of a LCD and the characteristics of a touch panel. The capacitive touch panel has been introduced in the Japanese and overseas markets as a display for smartphones and mobile devices, in which installation of the touch panel function has become indispensable since the spring of 2010.

The smartphone market is rapidly expanding, and the demand for large, high-resolution LCDs and capacitive touch panels is increasing. We are planning to meet this market need using our newly developed technology.

21-inch High-Resolution Autostereoscopic 3D LCD

21-inch high-resolution autostereoscopic 3D LCD

Toshiba Mobile Display Co., Ltd. has released a 21-inch high-resolution autostereoscopic three-dimensional (3D) LCD that realizes 3D images with a high degree of presence without the need for glasses, for application to next-generation TVs and monitors. The existing glasses-type system (two views) shows parallax images to each of the left and right eyes. On the other hand, the newly released 3D LCD utilizes the integral imaging method (ray reconstruction method) to show 3D images that are natural and smooth as if the real objects exist near the LCD.

The integral imaging method provides a horizontally wide viewing angle, and the 3D image remains smooth even when the viewer moves slightly in the horizontal direction. Therefore, the viewer does not feel fatigued even after viewing for a prolonged time, unlike the case of glasses-type systems. Furthermore, thanks to our low-temperature polysilicon (LTPS) technology, the 3D LCD maintains high resolution and high brightness with nine views.