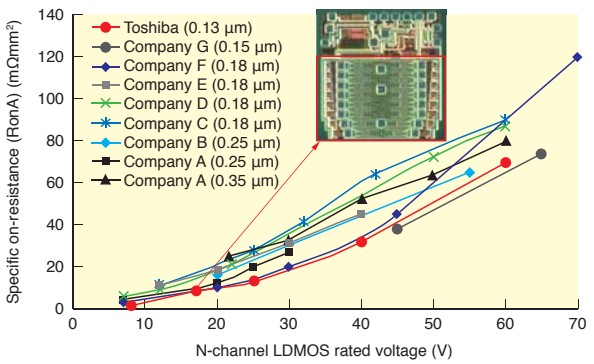
0.13 µm-Generation High-Voltage Analog-Mixed Process Technology



LDMOS: Lateral diffused MOS

Relationship between specific on-resistance (RonA) and rated voltage

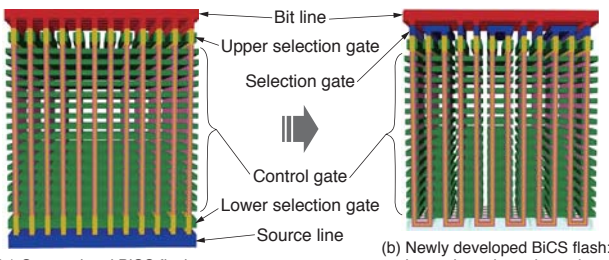
Toshiba has developed a 0.13 µm-generation BiCD(*) process, realizing one of the world's top-class high-voltage analog-mixed process technologies.

Its lineup comprises six types of lateral diffused metal-oxide-semiconductor (LDMOS) rated voltages: 8 V, 17 V, 18 V, 25 V, 40 V, and 60 V. This has been accomplished by mixing LDMOS having the optimal device design and impurity profile with 0.13 µm complementary MOS (CMOS) process technology. For the processes of 25 V or higher, a high-performance bipolar device is further embedded by isolating the device in such a way that a deep-trench structure is formed.

Our new technology also achieves one of the world's top-class performance in specific on-resistance, one of the LDMOS performance indexes.

As a result, in the 40 V series LDMOS, the device area has been reduced by 32% compared with our previous 0.35 µm-generation process.

(*) LDMOS embedded in a process in addition to bipolar transistors and CMOS



(a) Conventional BiCS flash: Linear transistor alignment

(b) Newly developed BiCS flash: horseshoe-shaped transistor alignment

Fig.2 Change from linear to horseshoe-shaped array structure to improve signal window and data retention

BiCS Flash Memory as Future 3D Nonvolatile Memory Technology for Ultrahigh-Density Storage Devices

Toshiba has developed the bit-cost scalable (BiCS) flash memory technology, which realizes three-dimensional (3D) memory with low cost and multilevel operation, toward further increasing the density of NAND flash memories to enlarge their capacity for use in portable digital equipment and solid-state drives (SSDs).

The BiCS flash memory utilizes our originally developed technology that produces an array of transistors in a 3D arrangement through a simple process as shown in Fig. 1.

The conventional BiCS flash memory, as shown in Fig. 2(a), has a problem of reduction of signals for memory operation and reliability deterioration, because of damage to the memory film during the fabrication process. An alignment of horseshoe-shaped transistors shown in Fig. 2(b) was therefore newly adopted to prevent damage to the memory film. This increases the signals, significantly improves the data retention characteristics, and makes multilevel operation possible. Using the new array structure of the horseshoe-shaped transistor alignment and 60 nm process technology, we fabricated a prototype 32 Gbit memory capacity test chip with a 16-layer memory cell, shown in Fig. 3, and verified the operation of a memory cell with an effective cell area of 0.00082 µm² per bit.

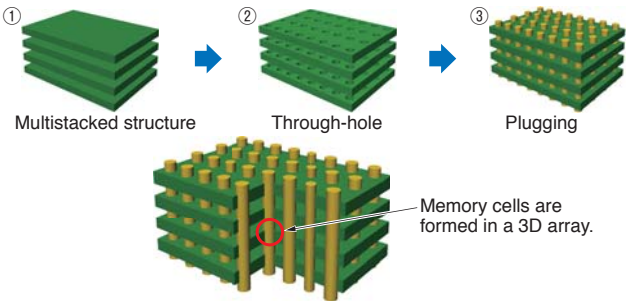
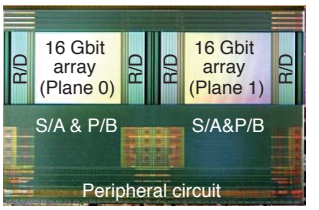


Fig.1 Concept of BiCS flash memory technology



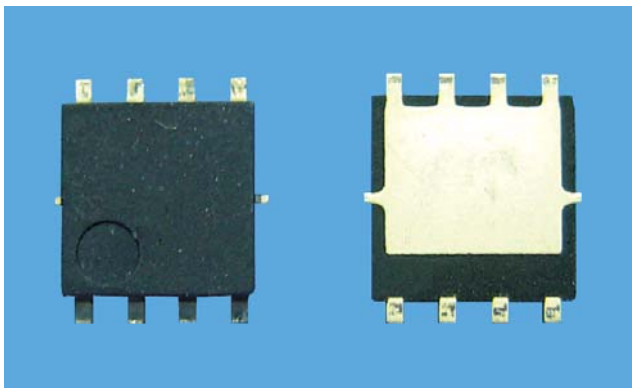
(a) Photo of test chip

(b) Cross-sectional scanning electron microscope (SEM) photo of cell (in manufacturing process)

R/D: row decoder
S/A & P/B: sense amplifier and page buffer

Fig.3 Fabricated 32 Gbit test array of 16-layer horseshoe-shaped BiCS flash memory with 60 nm technology

Seventh-Generation Series Low-Voltage Power MOSFET



"SOP Advance" package for low-voltage power MOSFETs

As mobile devices continue to offer higher performance while becoming smaller in size, further reductions in power loss and longer battery life are required.

In order to meet these market requirements, Toshiba has developed the seventh-generation low-voltage power metal-oxide-semiconductor field-effect transistor (MOSFET), in which the optimal balance is achieved among paradoxical characteristics such as lower on-resistance and high-speed switching by application of the latest trench structure.

Our new MOSFET will contribute to power loss reduction and downsizing of equipment through improvement of the figures of merit (FOM) by reducing the on-resistance (Ron) × gate switch charge (Qsw) characteristics, a performance index of MOSFETs, to approximately 83% compared with our conventional products.

This product will be developed into various compact packages to construct a lineup for a wide range of applications.

SDXC and SDHC Memory Cards with World's Fastest Read/Write Performance

64 Gbyte SDXC memory card

32 Gbyte SDHC memory card

16 Gbyte SDHC memory card

Toshiba has brought to market the world's largest capacity(*) SD memory cards: the 64 Gbyte SDXC memory card with the world's fastest read/write performance(*), and the 32 Gbyte and 16 Gbyte SDHC memory cards with the world's fastest read/write performance(*).

Digital cameras and camcorders require larger capacity SD memory cards for recording high-definition (HD) movies and still images, together with faster data read/write performance for high-speed continuous shooting or speedy copying to other media.

The three types of products developed this time offer a large capacity of up to 64 Gbytes, comply with the UHS104 card type defined in the SD Memory Card Specifications Version 3.0 for the first time in the world(*), and realize the world's fastest write performance of 35 Mbytes/s and read performance of 60 Mbytes/s.

(*) As of August 2009 (as researched by Toshiba)

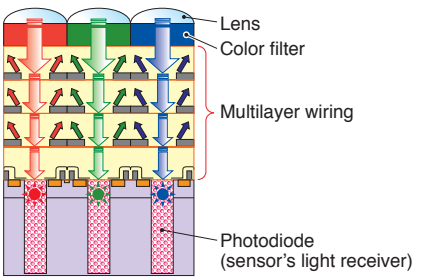
Dynastron™ BSI-Structured CMOS Image Sensor

Toshiba has developed the Dynastron™, a 14.6-megapixel CMOS image sensor that introduces a back-side illumination (BSI) structure enabling high sensitivity as a new type of CMOS image sensor.

Image sensors have the problem of decreasing sensitivity as the number of pixels increases. Our BSI-structured CMOS image sensor solves this problem by adopting design and process technologies to receive light from the back side so that the incident light does not attenuate in the wiring layer.

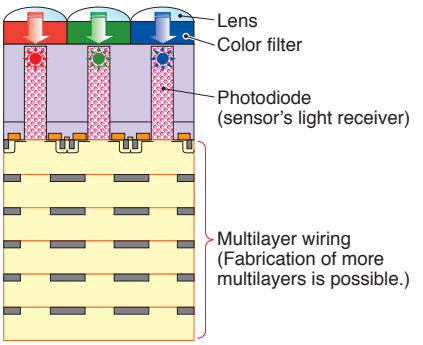
The newly developed product with a pixel pitch of 1.4 µm, one of the smallest in the industry, offers higher sensitivity compared with the same type of products without BSI technology.

The Dynastron™ will be applied to mobile phones and digital cameras in the future, utilizing its characteristics of high sensitivity and high-speed processing.



A wiring layer is formed above the light receiver and a lens is set over it. Since the light travels through the wiring, oblique light is obstructed and the sensitivity is weakened due to the reflection from the wiring.

(a) FSI



After the light receiver and wiring layer are formed, the lens is set close to the light receiver by grinding the substrate from the back side. For this reason, the sensitivity is increased without interference from the wiring.

(b) BSI

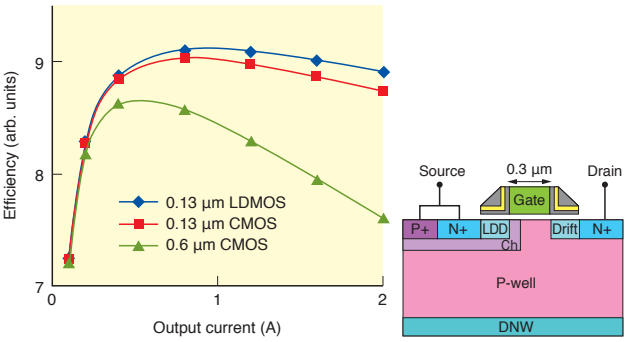
Comparison of device structures of conventional front-side illumination (FSI) image sensor and newly developed BSI image sensor

0.13 µm CMOS/LDMOS Platform Technology for Low-Voltage High-Frequency DC-DC Converters

Toshiba has developed a CMOS/LDMOS process platform based on 0.13 µm CMOS technology for analog and digital power applications. One of our targets is to develop a one-chip DC-DC converter. In particular, we are focusing on a low-voltage high-frequency DC-DC converter (maximum input voltage 6.5 V). The requirements for this high-frequency DC-DC converter are low cost, high efficiency, and large current driving capability.

In order to achieve high efficiency, we have developed low-voltage LDMOS with low specific on-resistance, low gate charge, and low gate-drain capacitance. Compared with the gate length of 0.6 µm of a 5 V CMOS with the same design rule to avoid the short channel effect, this 8 V LDMOS has a gate length of only 0.3 µm with the short channel effect suppressed even when the maximum gate operating voltage is 5 V. The obtained specific on-resistances of the 8 V N-channel LDMOS and 8 V P-channel LDMOS are 1.8 mΩmm^2 and 5.9 mΩmm^2, respectively.

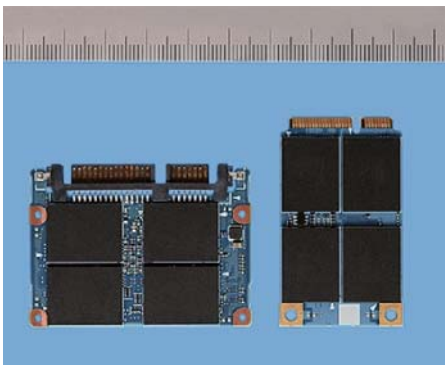
A comparison of simulated efficiency of the 5 V CMOS and 8 V LDMOS assuming that each chip has the same size of 1.1 mm×2.2 mm is shown in the figure, together with the efficiency of a CMOS with the previous-generation 0.6 µm design rule. Even in the case of large current driving capability, our 8 V LDMOS based on the 0.13 µm design rule maintains high efficiency, and half the loss of a CMOS based on the 0.6 µm design rule can be expected.



LDD: lightly doped drain
DNW: deep N-well

Comparison of simulated efficiency of LDMOS and CMOS assuming that each chip has the same size of 1.1 mm×2.2 mm

SSD Equipped with 32 nm Process Multilevel-Cell NAND Flash Memory



SSDs with 32 nm process multilevel-cell NAND flash memory

Lineup of SSDs equipped with multilevel-cell NAND flash memory

Toshiba has commercialized a 512 Gbyte SSD with the capacity of one of the largest class in the industry equipped with a 43 nm process multilevel-cell NAND flash memory for PCs.

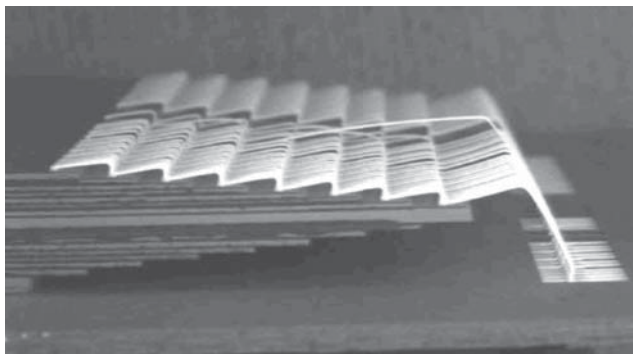
Its data processing speed is double that of existing products due to high-speed parallel reading/writing to the multilevel-cell NAND flash memories (maximum reading speed of 220 Mbytes/s, maximum, writing speed of 180 Mbytes/s).

Furthermore, by improving these technologies, we have commercialized the industry's first(*) compact, lower capacity type SSD equipped with a 32 nm process multilevel-cell NAND. Downsizing and power saving have been achieved in this product by utilizing a newly applied 32 nm process-compatible controller. It is approximately 1/7 the volume and 1/8 the weight of the conventional 2.5-inch type for PCs.

Our lineup of compact, low-power-consumption SSDs, as well as the large-capacity type, will be further enhanced and expanded in the future.

(*) As of September 2009 (as researched by Toshiba)

64 Gbyte *e*•MMC™ Embedded NAND Flash Memory with Industry's Largest Capacity



Internal structure of 64 Gbyte *e*•MMC™ embedded NAND flash memory

Toshiba has commercialized the 64 Gbyte *e*•MMC™, an embedded NAND flash memory with the largest capacity in the industry(*1).

This memory is equipped with a control function that encapsulates sixteen 32 Gbit NAND chips and a single controller chip in a small package conforming with the JEDEC Solid State Technology Association standard. High capacity is accomplished by 17-layer stacking, which was realized by employing 30 µm-thickness chip technology. Conformance with JEDEC version 4.4(*2) allows easy embedding in other applications and reduction of the user's development load.

A lineup of six types of products—64 Gbytes, 32 Gbytes, 16 Gbytes, 8 Gbytes, 4 Gbytes, and 2 Gbytes—is available to meet the demand for memories for portable devices.

(*1) As of September 2009 among embedded NAND flash memories (as researched by Toshiba)

(*2) One of JEDEC's embedded MultiMediaCard (MMC) standards for embedded NAND flash memory

e•MMC is a trademark of MultiMediaCard Association.

FDX4343R X-Ray Flat Panel Detector for Digital Radiography

FDX4343R X-ray flat panel detector for digital radiography

X-ray imaging detectors for diagnosis are rapidly shifting to digital image output. Toshiba Electron Tubes & Devices Co., Ltd. has released the FDX4343R(*), an X-ray flat panel detector for digital radiography, which converts input X-ray photons to digital still image signals.

The FDX4343R has a 143 µm-pixel thin-film transistor (TFT)/photodiode image sensor array with a detection area of 430 mm × 439 mm. This detector converts X-ray photons to light by means of a cesium iodide (CsI) scintillator screen deposited on an array of photosensitive pixels comprising a photodiode and a TFT switch. The FDX4343R simultaneously achieves high sensitivity and high resolution thanks to the use of a CsI deposition technology customized exclusively for flat panel detectors, a low-noise-readout IC and peripheral electronics, and highly effective light reflection layer technology.

By introducing these new technologies, the sensitivity has been improved by 50% while maintaining the same resolution. The FDX4343R also features packaging that is resistant to high humidity in order to safeguard its superior performance.

This detector is contributing to the progress of X-ray digital radiography technology due to its advantages of high sensitivity and high resolution while subjecting the patient to a lower X-ray dose.

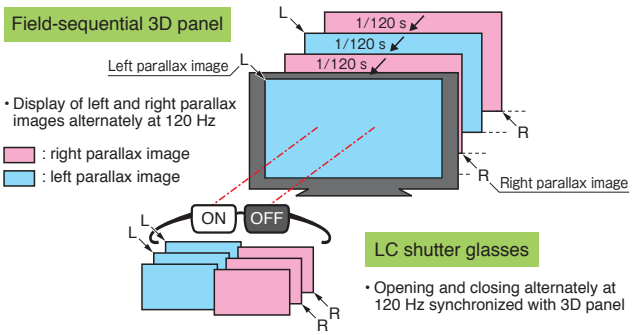
(*) The Pharmaceutical Affairs Act notification number 09B2X00009FPD002

3D Display with World's Highest Level of Image Quality

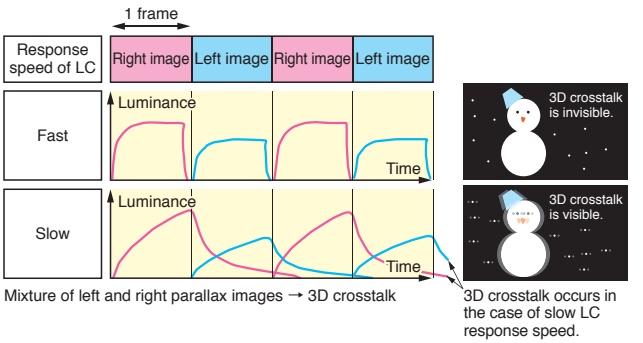
Toshiba Mobile Display Co., Ltd. has developed a high-quality stereoscopic display that overcomes the problem of 3D crosstalk, which refers to the level of mixing of the left and right parallax images.

Generally, a field-sequential stereoscopic liquid crystal display (LCD) for use with active shutter glasses, which alternately displays left and right parallax images, has the problem of 3D crosstalk because of the slow response of the LCs. To reduce 3D crosstalk, we have developed a new optically compensated bend (OCB) LCD with a response time of 3 ms. Furthermore, we have applied a black-insertion technology, which displays a black image between the left and right images, and a backlight-blinking technology. These technologies eliminate unwanted parallax images, achieving a 3D crosstalk ratio of 0.08% or less.

High-quality field-sequential stereoscopic displays with active shutter glasses are expected to become the mainstream in the 3D display market for TV systems and PCs. We believe that our 3D system providing the highest level of image quality will become the leading product in the 3D LCD market.



System of field-sequential stereoscopic display with glasses



Mechanism of 3D crosstalk occurrence