Corporate Research and Development

The Toshiba Group specifically focuses on the development of future technologies that serve as an engine of growth. The R&D Division is promoting the creation of new technologies including a next-generation battery technology, memory and storage technologies, and a host of others, as well as the enhancement of fundamental technologies and research and development contributing to current business activities.

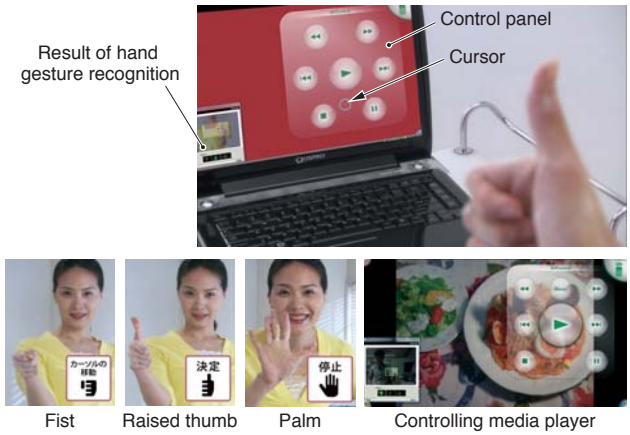
Video Processing Technologies on Toshiba's SE1000 Quad Core HD Processor

Toshiba has developed technologies for hand gesture recognition and video indexing taking advantage of the powerful video processing performance of our SE1000 Quad Core HD Processor.

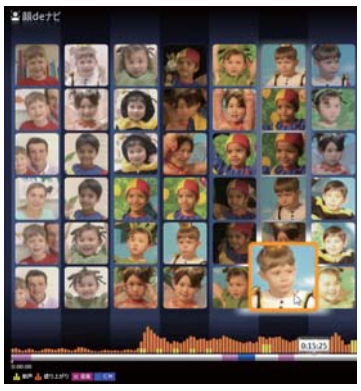
The hand gesture recognition technology detects three types of shapes of the user's hand (upper figure) in video images captured by a camera mounted on a PC. This technology makes it possible to control applications on the PC by hand gestures without the need for a mouse or a keyboard.

The video indexing technology detects faces, shouts, handclaps, commercials, music, and corner changes in recorded videos. Such information provides users with a novel way of watching videos by accessing favorite scenes using an overview of the videos such as thumbnails of the faces (lower figure).

HD: High definition



Operation of PC by hand gestures



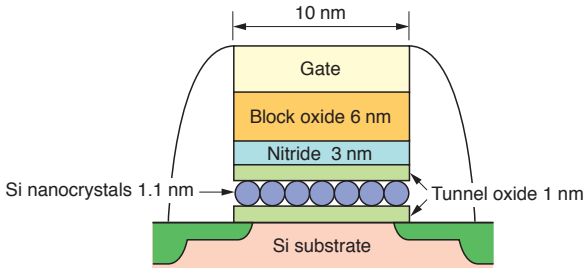
Accessing favorite scenes by face navigation

10 nm SONOS Type Memory Device Using Double Tunnel Junction

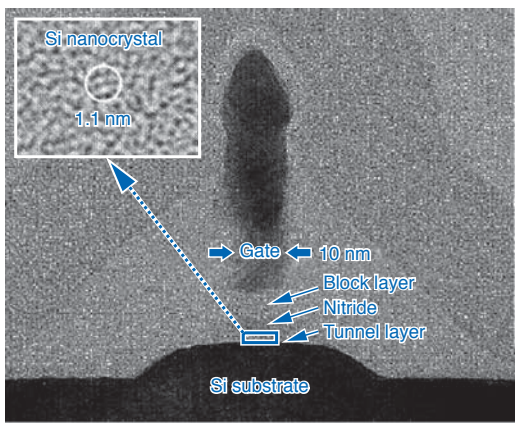
Toshiba has developed a new technology based on a silicon oxide nitride oxide semiconductor (SONOS) type memory structure having the potential for application to future 10 nm node flash memories, making it possible to realize the world's smallest(*) flash memory cell node. The technology also has the potential for even smaller nodes.

Toshiba achieved this by successfully fabricating an ultrathin, 1.1 nm silicon nanocrystal layer inside tunnel oxide films, using the advantageous characteristic that control of gate voltage can be employed to achieve large changes in tunnel resistance. This structure achieves the required levels of performance and reliability; namely, 10 years' data retention plus high-speed data writing and deletion. The most notable characteristic of the technology is that the smaller the silicon nanocrystals become, the higher the expectable memory performance. Since there is still room for miniaturizing silicon nanocrystals, this technology has prospects for applications below 10 nm; that is, at a single-digit nanometer node.

(*) As of December 2008 (as researched by Toshiba)



Memory device structure



Cross-sectional view of memory device

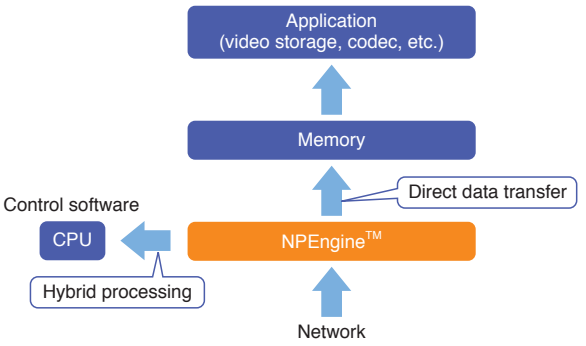
NPEngine™ Ultrahigh-Speed, Low-Power-Consumption TCP/IP Processing Engine

In future ultrahigh-bandwidth networks, the increase of network processing load on CPUs will be perceived as a problem. Toshiba has developed a hardware-based network processing engine called NPEngine™, which enables high-speed TCP/IP (Transmission Control Protocol/Internet Protocol) processing with very low power consumption.

A hybrid processing architecture in which data packets are processed by the hardware and other control packets are processed by software (host CPU, etc.) reduces the gate count. In addition, a direct data transfer technology eliminates the memory copy operation that has been a bottleneck in conventional systems, improving processing efficiency. NPEngine™ can achieve a TCP/IP throughput of about 1 Gbit/s with a system clock frequency of only 66 MHz, making it 10 times more power-efficient than a conventional software-based system. It can also achieve double the throughput with about half the gate count compared with a competitor's hardware-based system.

We plan to implement this system as a communication platform technology by further improving its throughput and adding support for more network protocols to be used in a wide range of networked equipment.

CPU: Central processing unit



Outline of packet receiving processing by NPEngine™

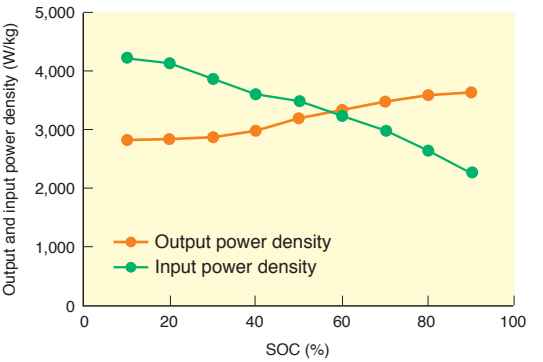
SCiB™ New High-Power Rechargeable Battery for HEV Application

SCiB™ battery for HEV

The market for rechargeable batteries for hybrid electric vehicles (HEVs) will continue expanding to meet the global demand for CO_2 reduction.

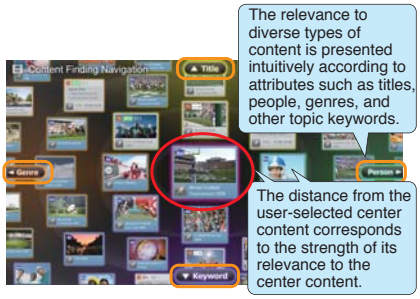
Toshiba has developed the SCiB™ high-power rechargeable battery with 3.3 Ah capacity offering high power performance, long life, and safety for HEV application.

The SCiB™ has flat power characteristics exceeding 2 600 W/kg in a wide state-of-charge (SOC) range of 20% to 80%, due to the use of a lithium titanium oxide (LTO) anode. Life performance between -40ºC and 60ºC was enhanced by avoiding the use of lithium metal plating on the LTO anode. The high-power and long-life characteristics of the SCiB™ make it possible to realize light and compact battery systems for HEV application.



Output and input power capability of SCiB™ for HEV application

"Content Finding Navigation" Content-Centric User Interface

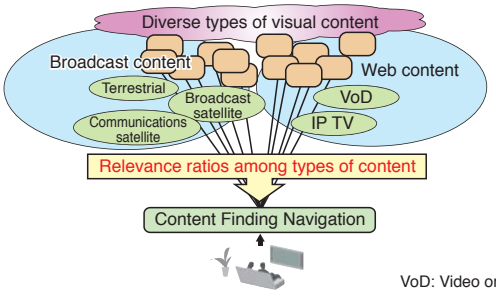


Screen image of Content Finding Navigation

Users can become overwhelmed by the vast amounts of visual contents available from various sources including digital terrestrial and satellite broadcasting, IP TV, and much more. Toshiba has developed a content-centric user interface called "Content Finding Navigation" that allows the user to swiftly discover the types of content corresponding to his or her interests in this ocean of visual contents. In order to offer seamless access to diverse types of broadcast media content, Content Finding Navigation provides a unified graphical user interface (GUI) based on relevance ratios among types of content. The relevance ratios of diverse types of content are calculated based on attributes such as titles, casts, categories, and other topic keywords.

Diverse types of media content are arranged in a three-dimensional (3D) space based on their relevance ratios, as shown in the upper figure. The distance between the user-selected center content and the other types of content corresponds to the strength of the relevance ratio. The direction between the user-selected center content and the other types of content represents reasoning attributes such as titles, people, genres, and other topic keywords. For example, content that is relevant to a cast member rather than other attributes is located in the direction of "Person."

This swift guidance interface based on the relevance ratios among types of content allows faster and easier access to the types of target content of interest. Furthermore, the user can discover types of content with the same cast or the same title that are scheduled to be rebroadcast. We intend to apply Content Finding Navigation to PCs and TVs as a unified GUI to support users' discovery of targeted contents.



VoD: Video on Demand

Concept of content-centric user interface

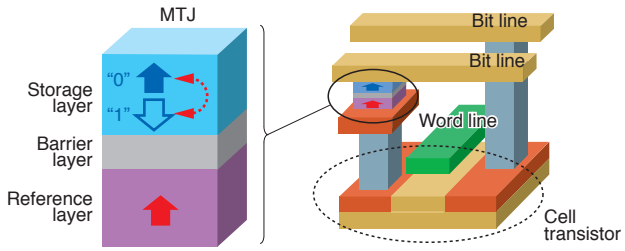
High-Density and Low-Power Spin-Transfer-Torque MRAM with Perpendicular MTJs

A magnetoresistive random access memory (MRAM) is a universal nonvolatile memory with fast read/write speed and unlimited endurance. So far, however, it has been impossible to design a Gbit-density MRAM.

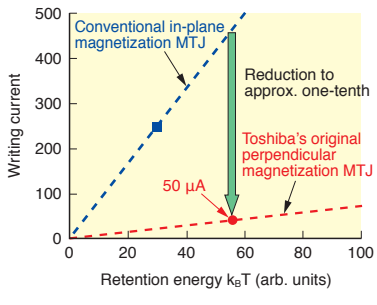
The most important issue in this regard is to significantly decrease the writing current. Toshiba has been developing a spin-transfer-torque writing technology with perpendicular magnetoresistive tunnel junctions (MTJs). We have successfully demonstrated a small writing current lower than 50 μA using our original perpendicular MTJs. This is the smallest current ever reported for nonvolatile MTJs. Further, fast writing with a writing current pulse of 4 ns has also been demonstrated.

These results have opened the way for the use of MRAMs in the main memory of PCs.

This work was partially supported by the New Energy and Industrial Technology Development Organization (NEDO).

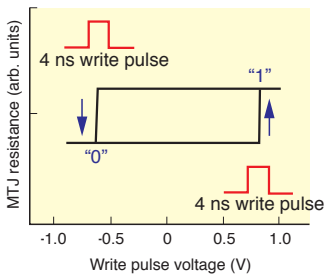


Schematic of element for perpendicular spin-transfer-torque MRAM



k_B: Boltzmann constant T: Absolute temperature

Technology for low writing current of less than 50 μA



High-speed switching in 4 ns writing

World-Record Quantum Key Distribution Bit Rate Realizing Ultra-Secure Networks

QKD system used in the EU field trial

Dramatic improvement in the performance and utility of quantum key distribution (QKD) will realize next-generation secure networks. Toshiba has increased the secure bit rate 100-fold, achieving values of 1.02 Mbits/s and 10.1 kbits/s over 20 km and 100 km of optical fiber, respectively. These are world-record values(*) and the first time that the bit rate has exceeded 1 Mbit/s under the unconditionally secure condition.

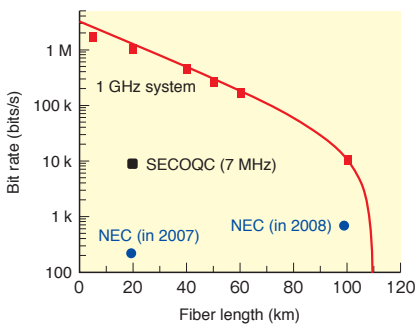
This advance stems from a recent invention by Toshiba Research Europe Limited (TREL) in the field of single photon detection technology. The self-differencing avalanche photodiode allows a 100-fold increase in the system clock rate and a 5 000-times higher maximum count rate.

We also participated in a field trial of a small-scale QKD network as part of the EU-funded SECOQC Project. Operating QKD in real telecom networks, as opposed to the private point-to-point links used previously, is essential to broaden applicability and lower cost. The TREL system (upper figure) operated stably and reliably during the month-long deployment. Following the successful conclusion of SECOQC, ETSI has launched a standardization initiative for QKD.

The recent increase in bit rate will allow QKD to be applied to much larger scale networks in the future. Higher bit rates are important because the key material must be shared between users in such networks. It will also extend the range of individual links and allow high-bandwidth unconditionally secure communications using a one-time pad.

(*) As of October 2008 (as researched by Toshiba)

SECOQC: Development of a Global Network for Secure Communication based on Quantum Cryptography
ETSI: European Telecommunication Standards Institute

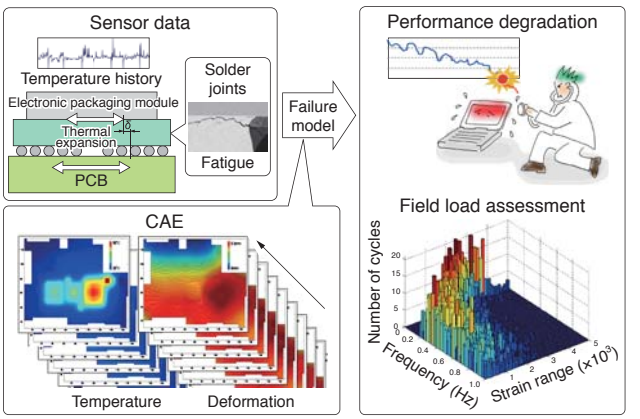


Comparison of final key rates for unconditionally secure QKD

Health Monitoring Technology for Printed Circuit Boards of Digital Products

Printed circuit boards (PCBs) of digital products such as notebook PCs are subject to cyclic loads of thermal stresses and external mechanical forces. Depending on the conditions of use, they may be at risk of performance degradation or unreliable operation.

Toshiba has developed a health monitoring technique for PCBs based on computer-aided engineering (CAE) that utilizes reliability test results. Cooling performance degradation and the field load history of a PCB are assessed by built-in sensors. This technology can lead to the reduction of downtime and leverage investigations to determine the cause of failure. Furthermore, the health monitoring data can be used as evidence in the design review process to ensure the required reliability of digital products.

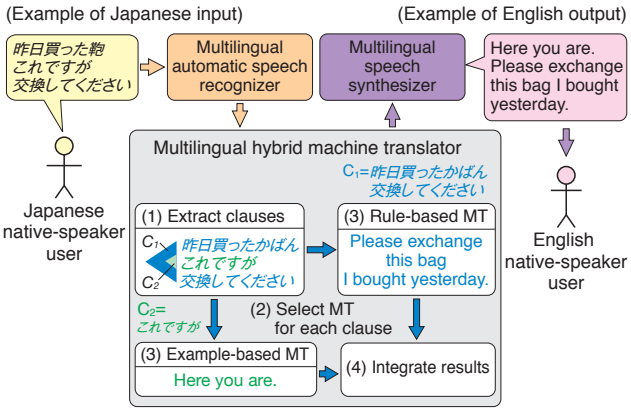


Flow of health monitoring for digital products

Full Six-Directional Japanese/ Chinese/English Speech-to-Speech Translator

Toshiba has developed a new hybrid translation method that realizes a speech-to-speech translator for all six translation directions among the Japanese, Chinese, and English languages. This hybrid method enables the system to produce natural and accurate translations for arbitrary spoken and recognized utterances. Two of Toshiba's original complementary machine translation (MT) methods are utilized: forest-driven rule-based MT, and chunk- and stochastic-type example-based MT.

Several field tests of this system were performed in Japan, China, and Australia in 2008, with participation by more than 130 native-speaking subjects for these three languages in total. The results of these field tests demonstrated that about 70% of typical tasks in overseas travel situations can be achieved within about two minutes.



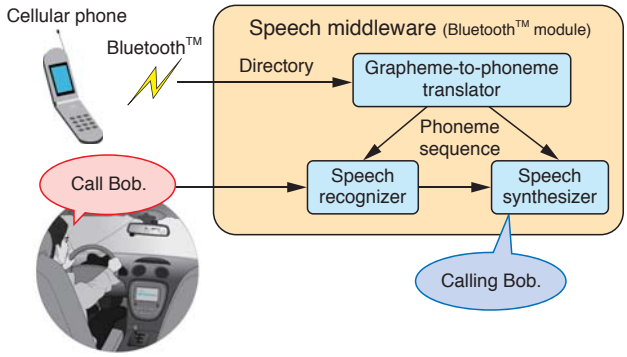
Configuration of Japanese/Chinese/English speech-to-speech translator

Speech Recognition and Synthesis Technologies on Bluetooth™ Chipset for In-Car Use

Toshiba has developed high-performance, small-footprint speech recognition and synthesis middleware on a Bluetooth™ chipset for an in-car hands-free communication system.

The speech recognizer achieves highly accurate speaker-independent recognition capable of recognizing continuous digits such as telephone numbers as well as commands even in a noisy environment, while the speech synthesizer produces highly natural and intelligible speech. A grapheme-to-phoneme translator is also provided, which can automatically produce phoneme sequences from name entries in directory information.

With the use of a Bluetooth™-enabled cellular phone, these speech technologies enable car drivers to make hands-free calls easily and safely simply by saying a person's name or telephone number such as "Call Bob" or "Dial 090 123 4567."



"Dial by voice" using speech recognition and speech synthesis technologies

The Bluetooth word mark and logos are owned by Bluetooth SIG, Inc. and any use of such marks by Toshiba is under license.

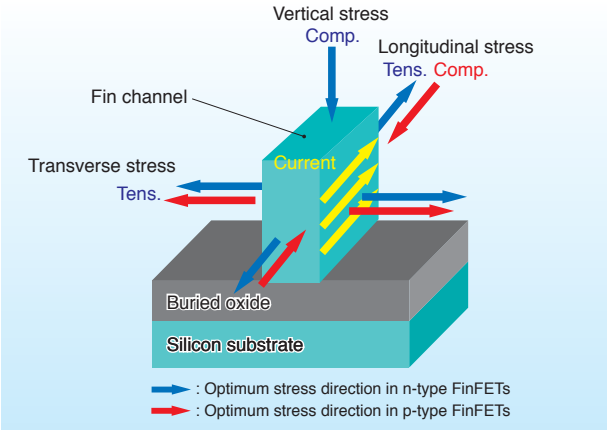
3D Stress Engineering in FinFETs for High-Performance LSI

3D transistors such as fin field-effect transistors (FinFETs) are promising device structures for next-generation logic LSIs, because they can reduce off-state leakage current and power consumption. However, a design guideline for a strained silicon channel in FinFETs to increase on-state drive current for high-speed LSI operation has not yet been clarified.

Toshiba has proposed a 3D stress engineering method in which transverse stress along the fin-width direction and vertical stress along the fin-height direction are introduced in addition to longitudinal stress along the gate-length direction of the FinFET. We have systematically measured the changes in carrier mobility by mechanically applying uniaxial stress to FinFETs, and clarified the types of stresses that should be applied along each direction to enhance mobility in n-type and p-type FinFETs.

This work was partly supported by the Innovation Research Project on Nanoelectronics Materials and Structures of the Ministry of Economy, Trade and Industry (METI).

LSI: Large-scale integration



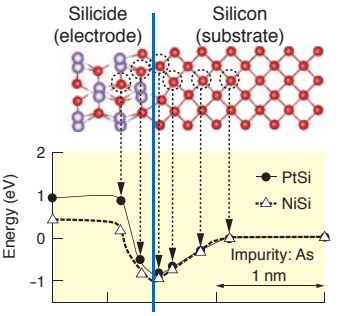
Tens.: Tensile stress
Comp.: Compressive stress

Optimum stress design in n-type and p-type FinFETs

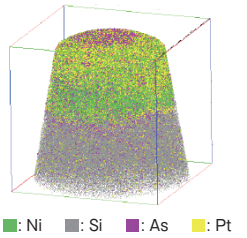
Low-Contact-Resistance Electrode Technology for High-Speed LSIs with Low Power Consumption

Reduction of the contact resistance of the interface between the metal electrode and silicon (Si) in Si transistors is of great importance to realize high-speed LSIs with low power consumption for the next generation.

Toshiba has studied dopant-migration behaviors around the interface between a platinum (Pt)-added nickel silicide (NiSi) electrode and Si, both theoretically with first-principle calculations and experimentally using the atom probe analysis technique. We have found that Pt segregated at the NiSi interface increases the interfacial concentration of both arsenic (As) and boron (B) dopants, leading to a dramatic reduction in the contact resistance. Based on this new finding, we have invented a new process with dopant implantation after NiSi formation, and have successfully reduced contact resistance by 50% in actual trials.



Energy of As in the substitutional site for Si at the interface of NiSi/Si obtained by first-principle calculation



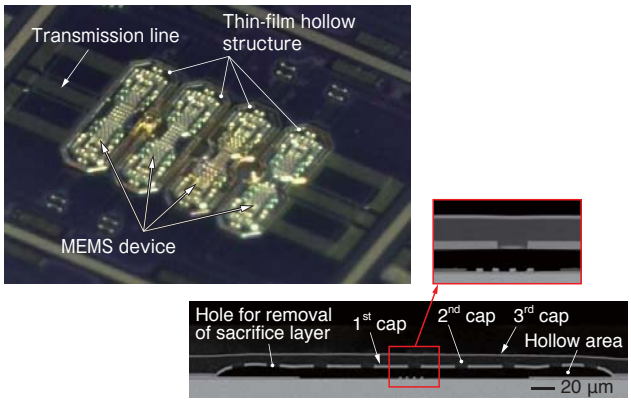
Distribution of As around the interface of NiSi/Si obtained by atom probe analysis

Analysis of As atoms at electrode-silicon substrate interfaces

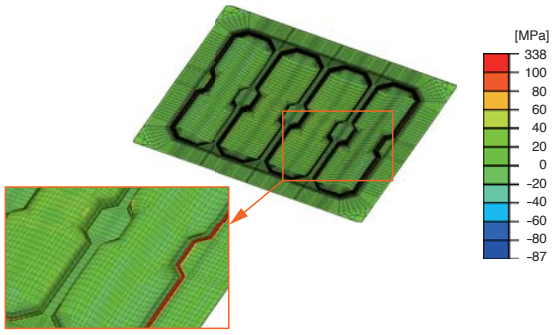
In-Line Wafer Level Package for RF-MEMS

Microelectromechanical systems (MEMS) can provide functions and characteristics that are difficult to realize in a semiconductor device. However, the market for MEMS is restricted due to the high cost of packaging to protect micro moving parts and so on.

Toshiba has developed two in-line wafer level packaging (WLP) technologies for MEMS that can achieve cost reductions. The first packaging technology covers encapsulation under atmospheric pressure conditions, and the second covers encapsulation under vacuum conditions. Applying these technologies to wafer level production through a front-end process, we have achieved the world's thinnest MEMS multichip package of 0.8 mm in thickness by stacking a driver IC chip and a MEMS chip with a thin-film hollow structure.



(a) Appearance and cross-sectional surface after encapsulation under atmospheric pressure conditions



(b) Optimization of structure by stress simulation

In-line WLP technology for radio-frequency MEMS (RF-MEMS)

High-Speed Die Bonder

High-speed die bonder

Toshiba has developed the world's fastest-class(*) die bonder, which will contribute to increased semiconductor package productivity.

This equipment picks up semiconductor device chips from wafers and mounts them onto lead frames. The newly developed bonder mounts multiple numbers of chips simultaneously, whereas previous models could only mount them one by one.

Thank to this new function, we have succeeded in reducing mounting time to 0.16 seconds per chip including the bonding process time. This performance was achieved by downsizing the mounting head and adopting a new chip position detection algorithm as well as a new lead frame transfer mechanism.

In addition, a force control mechanism that can quickly switch pressing force has been newly developed and implemented. This function helps to prevent the chips from being damaged.

(*) As of November 2008 (as researched by Toshiba)

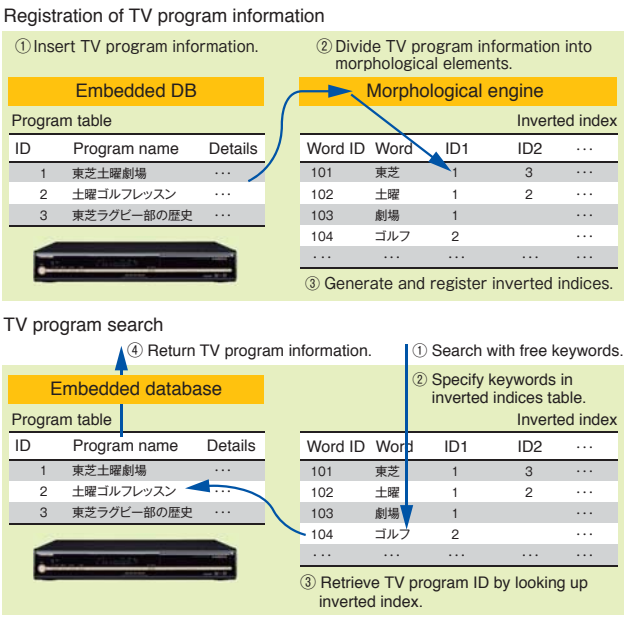
Advanced High-Speed Search Technology for TV Program Guide

Toshiba has developed an advanced search feature for TV program databases that allows users to freely enter keywords and retrieves related TV programs with high-speed performance. Moreover, this functionality has been successfully ported to a DVD recorder.

In systems developed so far, the search time increased proportionally with the number of programs in the program base. However, we achieved a high-speed, full text search function for electronic program guide (EPG) systems by administrating it with an open-source-based embedded database (DB). To realize the full text search function, the embedded DB was customized to generate inverted indices using morphological analysis.

Usually, full text search requires a large amount of memory, but we improved the system to make it work under limited memory conditions. Furthermore, the embedded DB was also customized to run in a fixed-size memory address space and file space.

Systems based on previous technologies could take up to 20 seconds from the beginning of the query to display of the result. Our technology shortens the time required to around one second. Furthermore, the embedded DB also includes functionalities to handle ambiguous expressions specific to Japanese writing.



ID: Identification

Outline of TV program registration and search

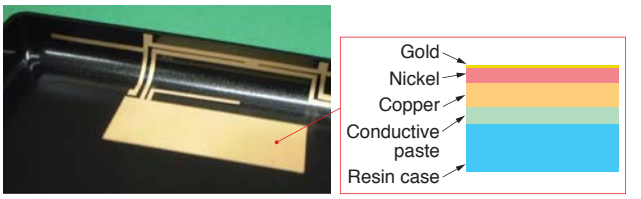
Technology for Circuit Forming on Resin Cases

Toshiba has developed a technology for forming circuits on resin cases, in which an electric circuit pattern is formed by printing conductive paste on the resin case and then plating the surface of the paste with metals such as copper. The main features of the newly developed technology are as follows:

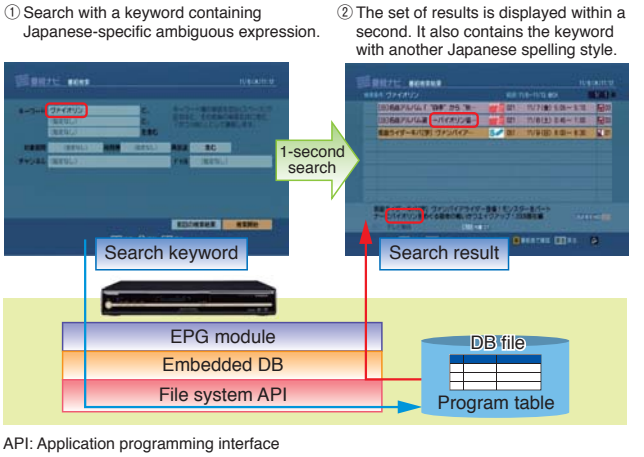
- The paste is cured at 70°C, which is below the thermal deformation temperature of the resin used for cases of mobile devices.
- The pad printing method is adopted, allowing the patterns to be applied to curved surfaces.
- The plating process used results in less damage to the paste.

The low-temperature-curing conductive paste was developed in collaboration with Toyobo Co., Ltd.

This technology can reduce the volume of antennas, which are increasing in size as functions expand in PCs and cellular phones. We are planning to establish mass-production technology for practical application of this circuit-forming technology in the future.



Antenna formed directly on resin case



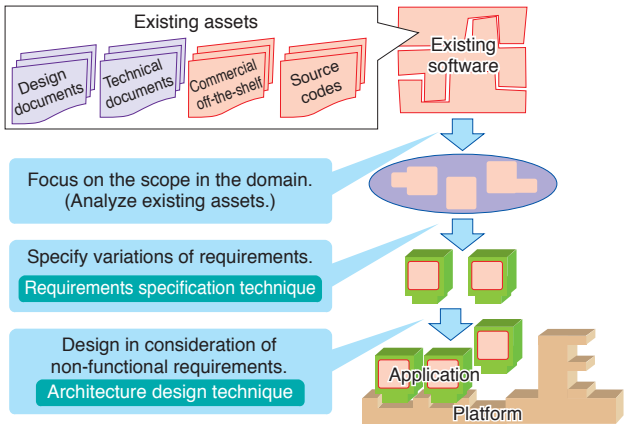
API: Application programming interface

Example of high-speed TV program search

Software Redesign and Software-Platform Reconstruction Technique

Software product lines for multiple customers and models have been increasing in recent software development. Construction of a software platform (SW-PF) can be an effective means of improving the productivity of software development. However, it may not be effective if the scope of the SW-PF and/or the results of analyzing software requirements are inappropriate. In such a case, it is necessary for the software developers to redesign the existing software based on the results of analyzing existing assets.

Toshiba has developed two core techniques for specifying variations of software requirements and design software architecture in consideration of non-functional requirements such as maintainability or portability. The reuse of assets that have been constructed using these techniques realizes efficient development of software products. At present, we are applying these techniques to the development of products in the digital products and social infrastructure systems fields.



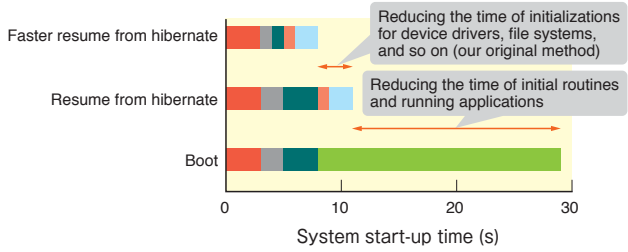
Software redesign and SW-PF reconstruction technique

Embedded Linux Fastboot Technology

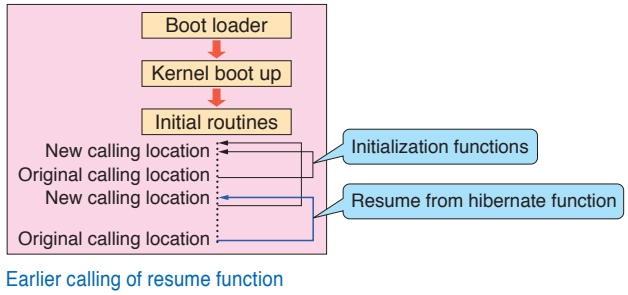
The hibernate function is seen in many operating systems where the content of RAM is written to nonvolatile storage such as the hard disk before powering off the system. The resume from hibernate is so fast that some embedded systems apply it for starting up the system.

Toshiba has developed Linux kernels that can resume faster from the hibernate state. We measured the system start-up time on a reference board for embedded Linux. The time for starting the system was reduced as follows: 30 seconds for boot were reduced to 13 seconds for resume from hibernate and further to 9 seconds for our faster resume from hibernate. Since our newly developed kernel calls the resume function earlier, we have succeeded in shortening resume from hibernate by about 4 seconds. This technology offers an original and versatile method independent of the specifications of devices and CPU architecture. We are now working on its practical application.

RAM: Random-access memory



Efficiency of faster resume from hibernate



Earlier calling of resume function

"Linux" is a registered trademark of Linus Torvalds in the United States and other countries.