# Electronic Components and Materials

In the electronic components and materials field, Toshiba focuses on the development of the key devices for new applications using an approach based on core cutting edge semiconductor process, design and applied technologies. We have produced a 56 nm CMOS multi-level cell NAND flash memory, a downsized CMOS area sensor achieved by reducing the pixel spacing, the world's thinnest and lightest LCD for mobile PCs, and so on.

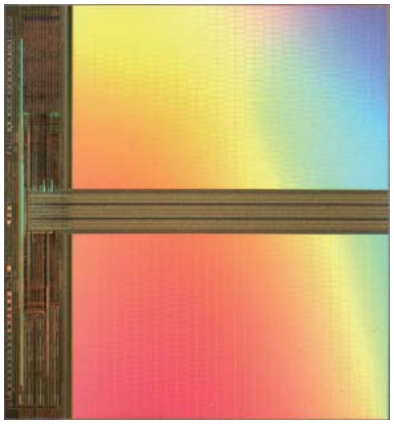
## 56 nm CMOS Multi-Level Cell NAND Flash Memory with High Programming Throughput

Toshiba has developed an 8-Gbit (1 Gbyte) single-chip, multi-level cell (MLC) NAND flash memory with state-of-the-art 56 nm process technology with the SanDisk Corporation, USA.

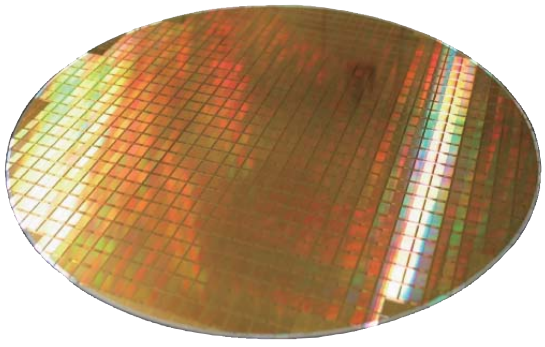
NAND flash memory is suitable for hand-held digital applications such as memory cards, USB memory, digital audio players and portable media players.

A higher density memory chip is preferable from a chip cost point of view. Both the circuit optimization and the advanced process technology make it possible to realize 30% smaller chip size than our previous 8-Gbit memory chip with 70 nm process technology.

Moreover, the adoption of MLC circuit technology and new memory cell array architecture offers high speed programming throughput at 10 Mbyte/s.



Micrograph of 8-Gbit NAND flash memory chip



300 mm wafer of 8-Gbit NAND flash memory

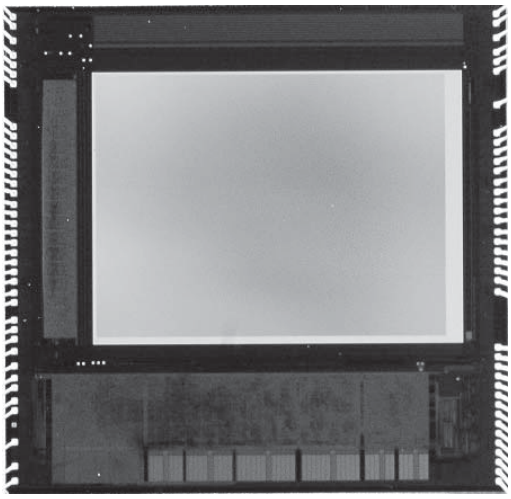
## Dynastron™ CMOS Area Image Sensor

Toshiba has newly developed and downsized two types of complementary metal-oxide semiconductor (CMOS) area image sensor Dynastron™, namely the 3.2-mega-pixel sensor ET8EE6-AS and 2.0-mega-pixel sensor ET8EF2-AS.

The pixel spacing of the newly developed sensors is considerably downsized from 2.7 µm to 2.2 µm reducing their total size, which was something for which there was great market demand in the field of camera modules for embedding in mobile devices including cellular phones. Accordingly, it was possible to downsize the optical formats of both the 3.2-mega-pixel sensor ET8EE6-AS and 2.0-mega-pixel sensor ET8EF2-AS to 1/3.2 inches and 1/4 inches, respectively from the previous 1/2.6 inches.

Both types offer all the advantages of CMOS area image sensors including smearless(*) imaging and high-speed operation. Their wide application in camera phones and other mobile devices is greatly expected.

(*) Smearless: free from the vertical stripes in an image that can occur when photographs are taken in bright light conditions, such as in direct sunshine.



Dynastron™, CMOS area image sensor

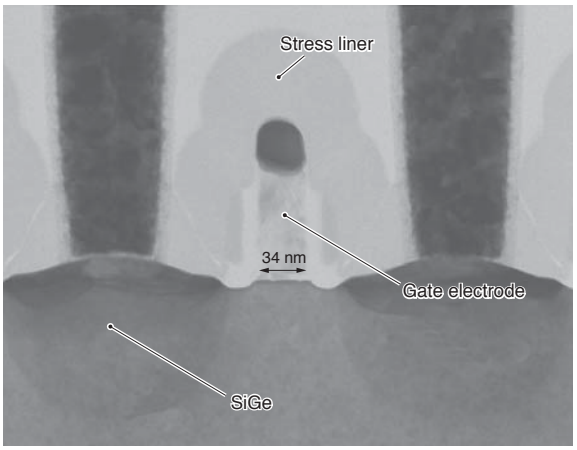
## A 45-nm High-Performance Bulk Logic Platform Technology (CMOS6) Using Ultra High NA (1.07) Immersion Lithography

Toshiba has developed a 45-nm high-performance bulk logic platform technology (CMOS6) and will start mass production based on this technology in 2008.

The ultra high NA (Numeric Aperture) (1.07) immersion lithography for a high-end logic process and advanced device-fabricating techniques were utilized to attain 70% miniaturization as compared with CMOS5 (65-nm process technology).

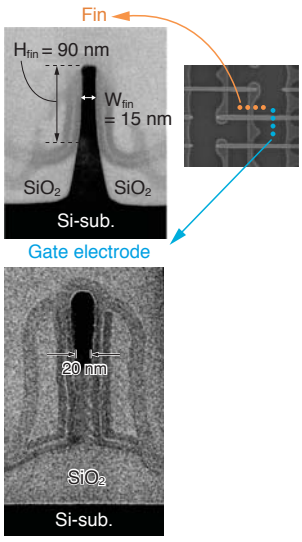
Stress control technology such as a DSL (Dual Stress Liner) approach, which applies reverse-direction stress by controlling the property of SiN films on both N-FET and P-FET, in the tensile strength direction and in the compressive stress direction, respectively, was utilized to upgrade transistor performance substantially by increasing the mobility of electrons and holes. Also, embedded SiGe (eSiGe) technology was used to increase the hole mobility in addition to the DSL approach.

In addition, a hybrid dual-damascene structure and a porous low-k interlayer dielectric (Keff = 2.7) were adopted to attain an approximately 50% reduction in chip area and 30% improvement in LSI operation speed as compared with CMOS5 (65-nm process technology).




P-type MOSFET fabricated with CMOS6 technology

## Bulk-FinFET SRAM Cell Technology for *hp*32 nm Technology Node and Beyond

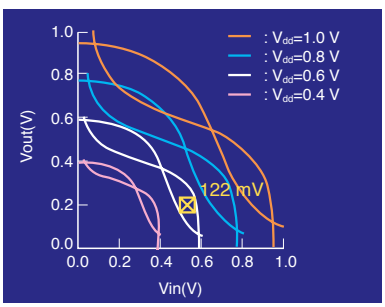



Cross sectional view of the FinFET SRAM cell

The FinFET is a kind of three-dimensional MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), in which the channel region is formed within the vertical surface of the Si pillar called "fin". The FinFET is a promising candidate for future CMOS devices in the *hp*32 nm technology node and beyond, because of its good cut-off characteristics and better punch through immunity by double gate mode operation. The FinFET fabricated on a bulk Si substrate (bulk-FinFET) in particular offers many advantages compared to a FinFET on an SOI (Silicon On Insulator) substrate, such as lower wafer cost and/or the ease of combination with conventional planar bulk CMOS devices. In this study, therefore, the combination of an SRAM (Static RAM) cell with the bulk-FinFET and the peripheral circuit with a conventional planar FET has been demonstrated on the same bulk-Si wafer.

In the experiment, FinFETs with a gate length down to 20 nm and fin width down to 15 nm were fabricated. The fin height was about 90 nm. Then, a bulk-FinFET SRAM cell array diagnostic monitor (ADM; 128 Kbit) is integrated and successfully operated for the first time. Higher β-ratio (β > 2.0) in the FinFET SRAM cell will also be achieved by tuning the effective channel width of each FinFET without area penalty. The measured butterfly curves show an excellent static noise margin (SNM) of 122 mV even at 0.6 V operation. Compared to the planar CMOS SRAM case, the FinFET SRAM cell will show larger stability, if the cell size is the same for both devices.

*hp*: half-pitch



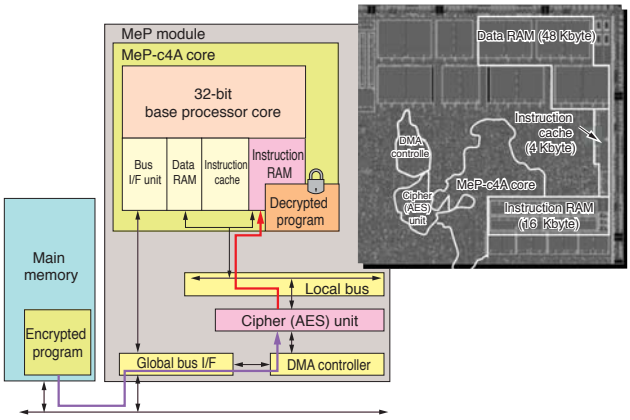

Butterfly curves for the FinFET SRAM cell

## MeP-c4A Security Enhanced Processor Core

Toshiba has developed a processor core called MeP (Media embedded Processor) -c4A that has the capability of protecting programs and reinforcing security function.

The MeP is a configurable processor embedded in the multimedia SoC (System on Chip) of digital appliances and cellular phones. An encrypted program on main memory that requires protection is decrypted during DMA (Direct Memory Access) transfer and the decrypted program is stored in the instruction RAM of MeP-c4. Under this condition, the program on the instruction RAM can only be executed, not read from or written to. Further, debug functions such as hardware breakpoints and trace functions are disabled, which protects the program against alteration and analysis. The program protection function is provided as a configuration of MeP-c4A.

Since functions to enhance security are becoming ever more important in multimedia SoCs recently, a variety of applications are expected for MeP-c4A.




I/F: Interface
AES: Advanced Encryption Standard

Block diagram of MeP-c4A processor core and example of layout

## 8 Gbyte SDHC Memory Card and Ultra High-Speed 4 Gbyte SDHC Memory Card


SD-HC008GT4/SD-HC004GT6

Toshiba has developed two new SDHC (SD High capacity) memory cards, the SD-HC008GT4 and the SD-HC004GT6.

The SD-HC008GT4 has capacity as large as 8 Gbyte, which is suited to movie/music recording. The card achieves class 4 performance which is equal to or faster than 4 Mbyte/s (*) performance. The maximum writing speed reaches 6 Mbyte/s.

The SD-HC004GT6 has 4 Gbyte capacity. The card achieves class 6 performance which is equal to or faster than 6 Mbyte/s (*) performance. The maximum writing speed is 20 Mbyte/s which is double the performance of Toshiba's previous high speed card.

(*) Under the conditions defined by the SD Card Association

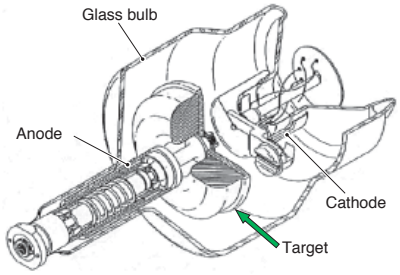
## High-Temperature Strength of Molybdenum Alloy Targets for X-Ray Tube Anodes

Molybdenum substrates for the rotating anodes of X-ray tubes or X-ray targets are required to have high strength at high temperature and low gas emission characteristics because they are used under vacuum at 1400 K. Conventionally, titanium-zirconium-composite-oxides-dispersion-strengthened molybdenum alloy substrates were used for X-ray targets, which however did not have sufficient strength at higher temperature although they had sufficient low gas emission characteristics. Toshiba has developed titanium-zirconium-composite-carbide-precipitation-strengthened molybdenum alloy substrates.

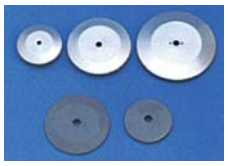
The new type alloy has around 1.2 times higher strength at high temperature as compared with the conventional alloy. It also has low gas emission characteristics based on our degassing technology. It is applicable for use in substrates for larger X-ray targets for high-powered X-ray tubes.

Strength of molybdenum alloy

| Mo alloy | Bending strength (MPa) | |
|---|---|---|
| | 293 K | 1873 K |
| Newly developed alloy | 850 | 151 |
| Conventional alloy | 750 | 129 |




Inside of an X-ray tube



Re-W/Mo targets

Re: Rhenium
W: Tungsten
Mo: Molybdenum

Appearance and high-temperature strength of molybdenum alloy targets for X-Ray tube anodes

## The World's Thinnest and Lightest(*) 12.1-Inch Wide-Format LTPS TFT LCD for Mobile Notebook PC Applications

Toshiba Matsushita Display Technology Co., Ltd has developed a 12.1-inch wide-XGA (1280×800) low-temperature poly-silicon (LTPS) TFT LCD for mobile notebook PC applications using a new light emitting diode (LED) backlighting system and a 0.2 mm thin glass substrate, and has started mass production of this product.

This approach has resulted in the development of the world's thinnest and lightest module(*) of 2.9 mm in thickness (at the thinnest part) and 183 g in mass which corresponds to about one-half the thickness and 32% lower mass compared with the current product using a cold cathode fluorescent lamp (CCFL) backlighting system, and the development of a mercury-free module which is environment-friendly.

(*) As of May 2007 (as researched by Toshiba)

New, lightweight TFT LCD, 12.1-inch wide format 2.9 mm thick