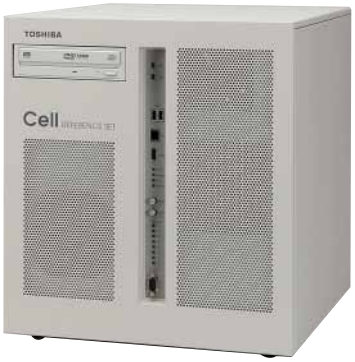
Electronic Components and Materials

In the electronic components and materials field, Toshiba proposes key devices for new applications while leading the field in cutting edge semiconductor device/process technologies. We provide a Cell Reference Set that offers an application development environment for the next generation multi core processor Cell, SoC (System-on-Chip) devices for digital AV applications and so on.

Cell Reference Set

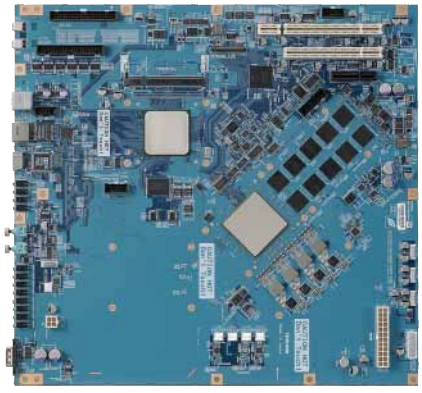


Cell Reference Set

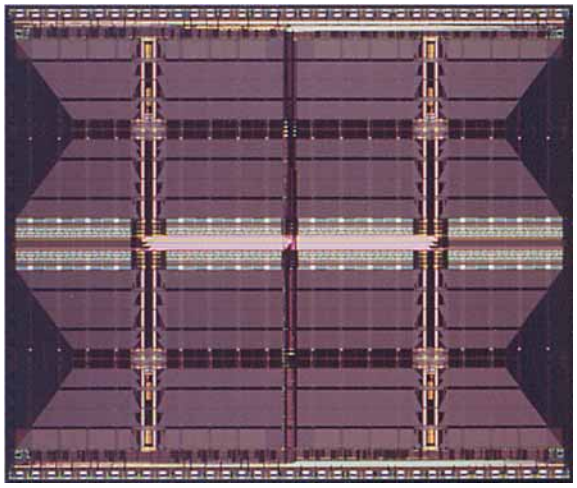
The Cell Reference Set (CRS) is an evaluation tool for the Cell Broadband Engine (CBE) and its chipset. The CRS is not only an ordinary microprocessor reference board, but also an audio visual (AV) computer provided in a chassis with all the basic and application software included in the set. The reason for using an AV application is to utilize CBE performance to the maximum extent and also demonstrate the CBE performance to the user visually. For the user the CRS offers the following three major advantages.

- The user can experience CBE performance with the AV demo application on the CRS.
- The user can develop and evaluate their application software on the CRS before starting actual development.
- The user can utilize CRS design documents in designing a product.

Use of the CRS clearly offers the user shorter evaluation and development time for their products and minimizes their risk.


Cell Reference Set main board

128 Mbit DRAM Using a Capacitor-Less DRAM Cell Called FBC


Micrograph of 128 Mbit floating body cell (FBC) DRAM

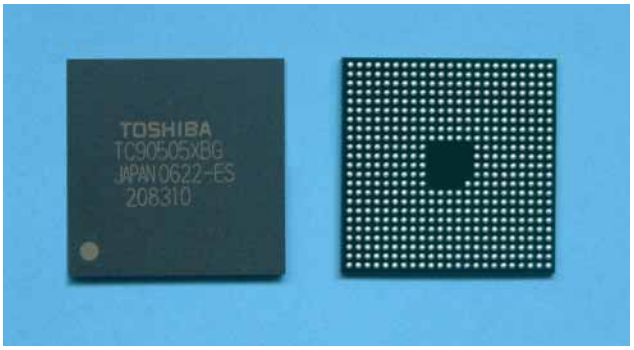
Toshiba has developed a 128 Mbit DRAM using a new memory cell called a floating body cell (FBC) which consists of a single MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) formed on SOI (Silicon On Insulator) in which the floating body serves as a data storage node.

Since the FBC has no capacitor, which is a key element in conventional DRAM cells and had become a major obstacle in reducing the size of the cell, it is possible for the new DRAM using the FBC to achieve memory with higher density and lower cost than that of existing DRAM. The new DRAM realizes memory fully compatible with conventional DRAM by eliminating data degradation problems due to charge pumping phenomenon, which are inherent in the FBC. The cell size is $6F^2$ (F is a minimum feature size) and the random access time is 18.5 ns at 25 ˚C.

Since the FBC is considered to be easily adaptable to the continuous miniaturization of semiconductor devices and it does not require overheads above those of the standard CMOS process, the memory is expected to be applicable for use in embedded memory in logic LSIs as well as high density stand-alone DRAMs.

The FBC also has the potential to achieve very fast access times and cycle times thanks to its small parasitic resistance and capacitance around the memory cell as well as its non-destructive readout and hence is expected to be a candidate memory cell for future high speed and high density embedded memory on SOI.

TC90505XBG Wireless LAN Baseband LSI for High-Definition A/V Content Transmission



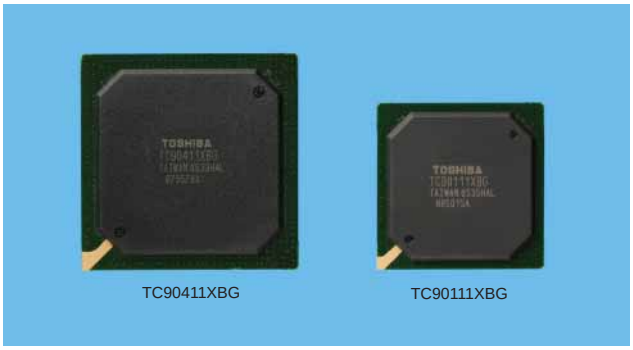
TC90505XBG wireless LAN baseband LSI for high-definition A/V content transmission

Toshiba has developed a wireless LAN baseband LSI (TC90505XBG) capable of transmitting high-definition audio with video (HD-A/V) content with secure content protection.

Thanks to the widespread proliferation of flat panel displays, wireless content transmission between a tuner and a separate display panel is attracting attention especially for wall-hanging TV or portable TV products. For this application, bandwidth sufficient to transmit HD-A/V content, robustness to permit stable communication in the home environment and content protection to prohibit casual copying are required.

To meet these requirements, the TC90505XBG not only fully complies with IEEE 802.11a, e, h, and i standards, but also supports original functionality. The HCCA (Hybrid coordination function Controlled Channel Access) mechanism of IEEE 802.11e ensures sufficient and stable bandwidth for transmission of HD-A/V content. The FEC (Forward Error Correction) mechanism is newly employed to attain both robustness and bandwidth requirements. As for copy protection, DTCP-IP (Digital Transmission Content Protection over the Internet Protocol) is implemented. An on-chip 64-bit RISC (Reduced Instruction Set Computer) processor operated at 240 MHz with hardware engine acceleration carries out protocol processing. PCI (Peripheral Component Interconnect), IIC (Inter Integrated Circuit)-bus and MPEG-2-TS (Moving Picture Experts Group-phase 2-Transport Stream) interfaces are also implemented for the convenience of connection to a TV system.

LSI Chip Set for Digital TV Receiver



TC90411XBG and TC90111XBG for digital TV

Toshiba has developed an LSI chip set, the TC90411XBG and TC90111XBG for digital TV receivers.

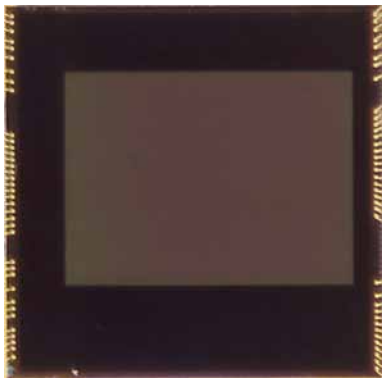
The TC90411XBG is a highly integrated LSI that realizes high definition processing with 1 chip. It incorporates a high performance host processor, an MPEG-2 decoder, a graphic engine, and an image-quality corrective controller. Moreover, our original configurable MeP (Media embedded Processor), which can be customized in function to suit the application is built in as a co-processor for audio and video decoding, and an increase in the efficiency of the system as a whole is attained by making the host processor concentrate on control of the whole system.

The TC90111XBG performs the interface function of high definition full digital HDMI (High Definition Multimedia Interface) input, and video input.

By using this chip set, a full HD 1080p(*) display becomes possible in a digital TV receiver.

(*) p: progressive scan

Dynastron™ 3.2-Mega-Pixel CMOS Area Image Sensor



Dynastron™ 3.2-mega-pixel CMOS area image sensor

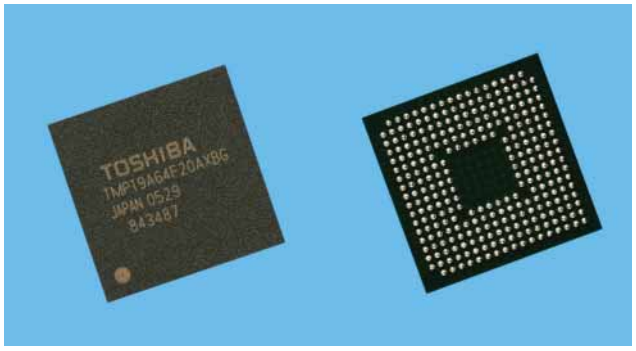
The 3.2-mega-pixel Dynastron™ (ET8E99-AS) has been developed aiming at further miniaturization and higher-resolution as a CMOS (Complementary Metal-Oxide Semiconductor) area image sensor for inclusion in mobile computing devices such as mobile phones with built in cameras.

This product achieves an optical format of 1/2.6 inches by greatly reducing pixel pitch from the current 3.75 µm to 2.7 µm.

The miniaturization of the camera module became possible as a result of reducing the size of the chip.

Furthermore, the quality of the image has been improved by the optimum design of micro lens and photo-diode.

32-Bit RISC Microcontroller with NANO FLASH™ Memory



TMP19A64AF20AXBG 32-bit RISC microcontroller

Toshiba has developed a new 32-bit, single-chip MIPS-based™ RISC MCU (Micro Controller Unit) TMP19A64AF20AXBG with on-chip NANO FLASH™ memory, which realizes fast program and erase times with low power consumption.

The TMP19A64AF20AXBG integrates 2 Mbyte NANO FLASH™ memory and 64 Kbyte random access memory and includes among its many functions a 24 channel analog-to-digital converter, an 8 channel high-speed serial interface and other peripheral interfaces.

The MCU is capable of controlling a large program with a single chip and is ideal for portable digital consumer applications.

Toshiba NANO FLASH™ is a new technology for embedded MCUs that combines a NAND flash memory cell and a NOR flash memory peripheral circuit to create high-density embedded memory. The NANO FLASH™ achieves around the same low power consumption as that of embedded mask ROM.

"MIPS-based" is a trademark of MIPS Technologies, Inc.

Small Fuel Cell for Mobile Audio Applications

Prototype DMFC-powered gigabeat™

Prototype DMFC-powered cellular phone (jointly developed with KDDI)

Toshiba has developed a small passive type direct methanol fuel cell (DMFC) that is suitable for use as a power supply for handheld electronic devices. The DMFC units were integrated into prototype HDD-based audio players (gigabeat™), and the field test to validate their performance has begun.

Through durability and reliability tests, Toshiba will accelerate technology enhancements, including the development of production technologies, to support the integration of DMFCs into commercial products.

The prototype audio player and prototype DMFC embedded cellular phone (jointly developed with KDDI) were exhibited at CEATEC JAPAN 2005.

Input Display with Pen and Finger Input Functions

Toshiba Matsushita Display Technology Co., Ltd. has developed an input display which allows input operation to be performed using either a finger or a light pen.

System-on-glass (SOG) technology, which utilizes the characteristics of low-temperature polysilicon, has enabled us to integrate optical sensors and signal processing functionality directly into the glass substrate of a liquid crystal display (LCD). Thus, this input display eliminates the need for the attachment of other components such as a touch panel as is conventionally required, and is expected to find applications in portable/mobile devices, which demand thinner, smaller, and lighter displays with greater reliability.

This development is a further improvement to the world's first input display (an LCD capable of capturing images of objects placed on top of it), which we announced in April 2003.

Item	Specifications
Display size (diagonal)	6.1 cm (2.4 in)
Pixel format	240 × 320 (QVGA)
Number of color display, mode	65 K colors, transmissive
Display refresh rate	60 Hz
Reading data rate	60 Hz

Display with integrated touch panel function

Item	Specifications
Display size (diagonal)	8.9 cm (3.5 in)
Pixel format	320 × 240 (QVGA)
Number of color display, mode	260 K colors, transmissive
Display refresh rate	60 Hz
Reading data rate	60 Hz

Display with integrated pen input function