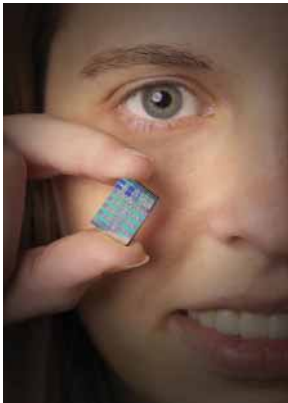


Toshiba is focusing on developing the key devices such as mobile tools and digital home appliances that will support the ubiquitous network society. Namely, next-generation advanced Cell microprocessors and high-performance SoC (System-on-Chip) devices. Moreover, we will offer display devices that ensure fast response, wide viewing angle and clear moving video pictures for next-generation flat panel displays.

## IBM, Sony, Sony Computer Entertainment Inc. and Toshiba Disclose Key Details of the Cell Chip



The Cell chip

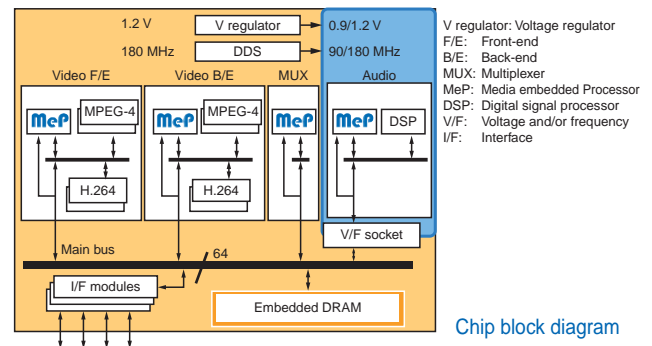
At the ISSCC 2005 (International Solid State Circuits Conference 2005), IBM, Sony Corporation, Sony Computer Entertainment Inc. (Sony and Sony Computer Entertainment collectively referred to as the Sony Group) and Toshiba Corporation (Toshiba) for the first time disclosed in detail the breakthrough multi-core architecture design – featuring supercomputer-like floating point performance with clock speeds greater than 4 GHz observed in the laboratory – of their jointly developed microprocessor code-named Cell.

A team of IBM, Sony Group and Toshiba engineers has been collaborating on development of the Cell microprocessor at a joint design center established in Austin, Texas, since March, 2001. The prototype chip is 221 mm<sup>2</sup>, integrating 234 million transistors, and is fabricated with 90 nm SOI (Silicon on Insulator) technology.

Cell's breakthrough multi-core architecture and ultra high-speed communication capabilities deliver vastly improved real-time response for entertainment and rich media applications, in many cases 10 times the performance of the latest PC processors.

Effectively a "supercomputer on a chip" incorporating the advanced multi-processing technologies used in IBM's sophisticated servers, Sony Group's computer entertainment systems and Toshiba's advanced semiconductor technology, the Cell will become the broadband processor used for industrial applications in the digital home of the future.

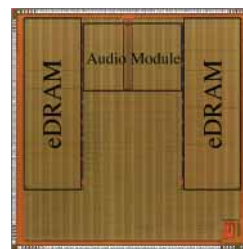
## 63 mW H.264/MPEG-4 Audio/Visual Codec LSI with Module-Wise Dynamic Voltage/Frequency Scaling



Toshiba has developed a single-chip H.264 and MPEG-4 (Moving Picture Experts Group-phase 4) audiovisual LSI for mobile applications including a terrestrial digital broadcasting system with a module-wise, dynamic voltage/frequency scaling architecture. This LSI has an architecture that uses a microprocessor with dedicated accelerator circuit modules and an embedded DRAM, as shown in the figure (top). The audio module is isolated in a separate domain under independent control for voltage and frequency. This LSI can keep operating even during voltage/frequency transition, so there is no performance overhead. This is realized through the use of a dynamic deskewing system (DDS) and an on-chip voltage regulator with skew rate control. By working in combination with traditional low power techniques such as embedded DRAM and clock gating, it consumes only

116 mW in encoding VGA (640×480) MPEG-4 video at 30 frames/s and MPEG-4 AAC LC audio, and 63.3 mW in decoding QVGA (320×240) H.264 video at 15 frames/s and MPEG-4 AAC LC audio simultaneously.

The chip micrograph is shown in the figure (left). Chip features are shown in the table (bottom).

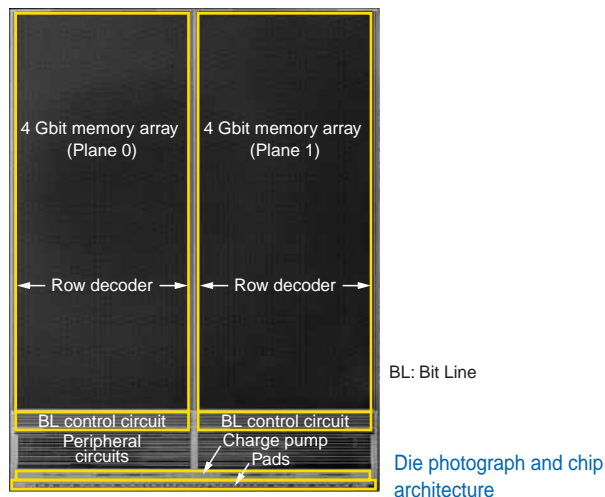


Chip micrograph

### Chip features

Technology	90 nm CMOS
Operating frequency	180 MHz/90 MHz (audio at low speed)
Video format	H.264 baseline profile at Lv 2, MPEG-4 SP@L4a
Video performance	H.264 CIF 30 frames/s decode, MPEG-4 VGA 30 frames/s encode/decode
Audio format	MPEG-4 AAC LC, MP3
Speech format	AMR, G.726
Demultiplex format	MPEG-2 TS

## 8 Gbit NAND Flash Memory with 70 nm CMOS Technology



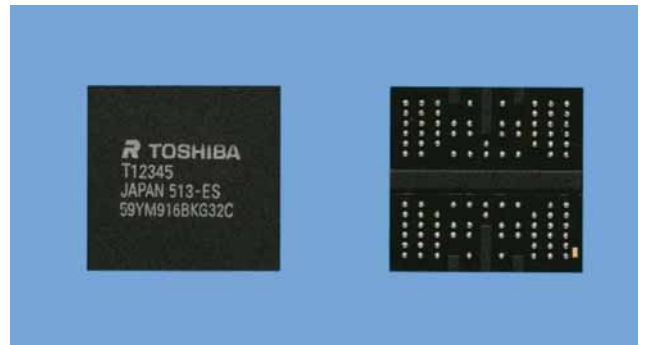
The continuous bit cost reduction with increasing flash memory die-densities has expanded the variety of portable mass data storage applications such as digital still cameras, cellular phones, USB memory, portable audio and video.

Toshiba has developed a 145.5 mm<sup>2</sup>, 8 Gbit multi-level cell (MLC) NAND flash memory with 4-level programmed cells and cost-efficient chip architecture with a 70 nm CMOS process technology, which is the highest flash memory density reported to date. Both control and I/O pads are located at the bottom of the chip arranged in one row. This pad arrangement reduces the pad area by half compared with previous generations. Also, the area of power lines and signal wiring is smaller than that of conventional units thanks to the simple core design. Overall, a highly cost effective, 73.5% of memory cell efficiency has been achieved. Since the main circuits are located close to the bottom of the chip, the data path is shortened, which enables fast, synchronous burst operation.

The chip is fabricated with a 70 nm p-sub triple-well CMOS process with 3-metals. The power supply voltage is 3.3 V. With innovative circuit implementation such as write cache and programming voltage control, 6 Mbyte/s throughput for MLC programming has been achieved, which is significantly faster than ever previously reported, and very competitive with binary flash memory. The read throughput is as fast as 60 Mbyte/s with  $\times 16$  bit I/O option.

Source from ISSCC 2005, pp.44-45 and the IEEE copyright

## 512 Mbit XDR™ DRAM 4.8 GHz Data Transfer Speed

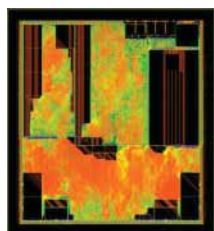


High-speed 512 Mbit XDR™ DRAM

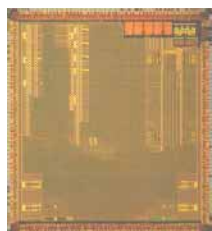
512 Mbit XDR™ DRAM with a data transfer speed of 4.8 GHz per pin is the world's fastest memory device. XDR™ DRAM is designed for high-performance broadband applications, including digital consumer electronics, network systems and graphics systems. The XDR™ DRAM is based on Rambus' XDR™ memory interface technology and offers eight times the bandwidth of today's best-in-class PC memory. The XDR™ DRAM uses differential Rambus signaling levels (DRSL) for scalable high speed point to point bi-directional data signals and Rambus signaling levels (RSL) for source synchronous bussed address and command signals to control multiple DRAM devices. The point to point connected data bus allows multi GHz speeds while the bussed addresses and commands allow scalable capacity of multiple DRAM devices per requested bus channel. The combination of DRSL and RSL signaling provides a low cost and high performance interconnection solution for applications demanding high bandwidth. Octal data rate (ODR) allows eight bits of data to be read from and written to DRAM in a single clock cycle, and the 600 MHz clock cycle delivers data at a 4.8 GHz per pin rate which allows a typical  $\times 16$  bit I/O device to sustain 9.6 Gbytes per second bandwidth per chip. The 512 Mbit XDR™ DRAM is built on the 110 nm DRAM process and it is available in the 108 (100) ball molded BGA (Ball Grid Array) package.

"XDR" is a trademark or registered trademark in Japan and/or other countries.

## Industry's First SoC with X Architecture for Production



Pattern layout plot of SoC with X Architecture



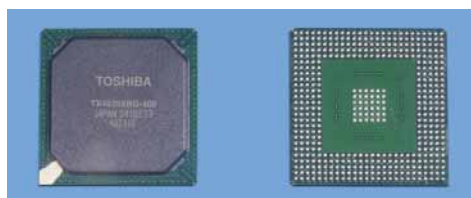
Micrograph of SoC with X Architecture

Toshiba has developed the industry's first commercial system-on-chip (SoC) devices built on the innovative X Architecture.

The X Architecture is a new method of implementing a chip by using 45 degree or 135 degree diagonal wires in addition to the traditional right-angle "Manhattan" routing. This innovative architecture enables the production of smaller, faster chips. Toshiba and Cadence Design Systems, Inc. have collaborated on the development of this new technology.

The milestone chip, TC90400XBG, is for digital TV applications initially for the European market. As compared to the conventional "Manhattan" design, the TC90400XBG applying the X Architecture is approximately 11% faster in speed and 10% smaller in random logic area.

## Highly Integrated 64-Bit RISC Microprocessor for Digital Consumer Applications



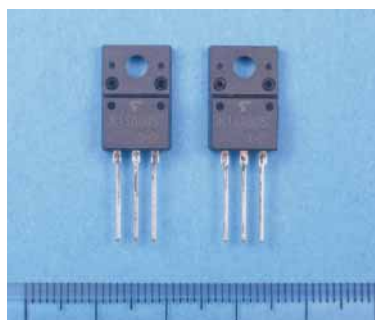
TX4939XBG-400

Toshiba has developed a new 64-bit single chip MIPS-based™ RISC (Reduced Instruction Set Computer) microprocessor, the TX4939XBG-400, that uses the industry-leading 90-nm process technology and the proprietary TX49/H4 400-MHz operating frequency CPU core.

The TX4939XBG-400 is targeted at diverse digital consumer applications.

It blends processing power and the rich feature set required for digital consumer applications by integrating

## High Voltage DTMOS Power MOSFET Uses Super Junction Structure



Outline of the TK15A60S

Toshiba has developed a new power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) called DTMOS (Deep Trench MOSFET). DTMOS employs a new super junction structure that enables a reduction in power consumption caused by on-state resistance ( $R_{DS(on)}$ ) to approximately 40% of the value typically achieved with conventional MOSFETs.

The First device in the DTMOS family, TK15A60S, is targeted for use in power supplies for television sets, home appliances and AC adapters.

The super junction structure, which has vertical paths to allow electrical current to flow through easily on a silicon substrate, realizes lower  $R_{DS(on)}$  than the theoretical limit of silicon. By applying this super junction structure and optimizing the device as a whole, the  $R_{DS(on)}$  for the same area in Toshiba's DTMOS device achieves a 60% reduction and its gate charge ( $Q_g$ ) achieves a 40% reduction compared with Toshiba's conventional MOSFETs. Consequently,  $R_{DS(on)} Q_g$ , a characteristic that is an important performance index for MOSFETs (the smaller the better), is one quarter the value of the company's conventional MOSFETs.

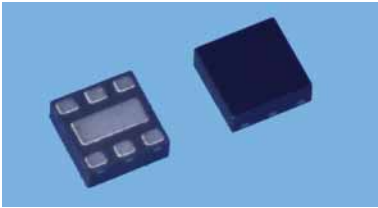
a high-performance security engine, serial and parallel video ports, battery back-up support, multiple hard disk interfaces, a DDR SDRAM controller and Ethernet controllers.

The chip is assembled in a small thin 456-pin BGA package (27 mm×27 mm).

With its multiple on-chip peripheral functions, our new TX4939XBG-400 lowers system cost and reduces development time for customers.

DDR SDRAM: Double Data Rate Synchronous DRAM

## TG2217CTB Super Small GaAs SPDT RF Switch



TG2217CTB super small GaAs RF SPDT switch

Toshiba has developed a super small and super low profile gallium arsenide (GaAs) metal-semiconductor field effect transistor (MESFET) SPDT (Single Pole Dual Throw) RF switch, the TG2217CTB.

The development of cellular handsets is headed toward the support of multiple applications such as Bluetooth™ and GPS (Global Positioning System), and the accommodation of multiple communication formats such as GSM and W-CDMA in order to be compatible with wide-range international roaming. This has resulted in a tendency toward complicated circuit structures and an increase in the number of switches and other components, which intensifies the need for downsizing.

In response to these needs, Toshiba has realized a mounting area 45% of that of previous products and a low profile of 0.38 mm by adopting lead frame chip scale package (LF-CSP) technology\* with no sacrifices in electrical characteristics.

This SPDT switch operates at up to 3 GHz requiring two control positive voltages also acting as bias supply. The control voltages are very low and 2.4 V operation is possible. This enables compatibility with the trend toward lower voltages for baseband LSI.

This product contributes significantly to the downsizing and low-voltage operation of various RF (Radio Frequency) products.

W-CDMA: Wideband Code Division Multiple Access  
GSM: Global System for Mobile communications

\* LF-CSP technology: A technology that realizes high-density packaging by mounting chips on a lead frame which forms the pads.

### Specifications of the TG2217CTB

Characteristics	Specifications
Voltage range	Vc(H)=2.6 V (typ.), Vc(L)= 0 V (typ.)
Input power at 1 dB compression point	17 dBmW (typ.) at 2.5 GHz
Insertion loss	0.35 dB (typ.) at 1 GHz
Isolation	24 dB (typ.) at 1 GHz
Operation temperature	-40°C to 85°C
Packaging	6-pin CSP (1.0 mm×1.0 mm×0.38 mm) Pb-free package

"Bluetooth" is a trademark owned by Bluetooth SIG, Inc., U.S.A.

## Next-Generation Flat Panel Display "SED"



36-inch diagonal WXGA SED

Toshiba, in collaboration with Canon Inc., has developed a 36-inch diagonal WXGA SED (Surface-conduction Electron-emitter Display).

The SED displays an image using the fluorescence of phosphors hit by electrons emitted from a surface-conduction electron-emitter, which utilizes a tunneling phenomenon at gaps of a size in the order of nanometers produced by original technology.

Based on the same light-emitting principle as the cathode ray tube (CRT), the SED inherits the highly reputed picture quality of the CRT but with improvements in sharpness and other characteristics.

The main characteristics of the 36-inch diagonal WXGA SED are as follows:

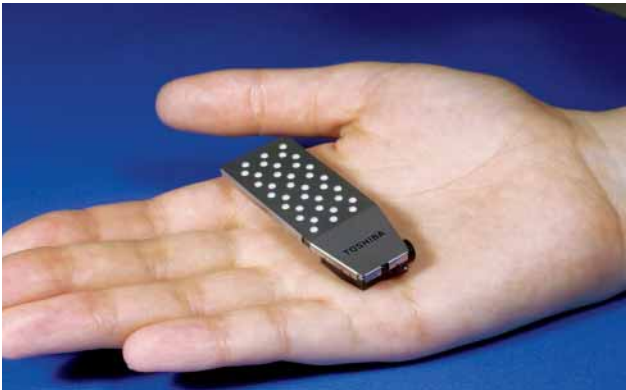
- High dark room contrast ratio (approximately 100,000:1)
- Good response to moving pictures (the same as CRT)
- Low power consumption (135 W at APL= 0.25)

From now, SED Inc., a Canon-Toshiba Joint Company, established last year, will begin pilot production of 50-inch class HD panels. Then, mass production will be begun and the lineup expanded.

WXGA: Wide extended Graphics Array (1,280×768)  
APL: Average Picture Level



## World's Smallest Direct Methanol Fuel Cell System



The world's smallest direct methanol fuel cell system

Toshiba has developed the world's smallest passive-type direct methanol fuel cell (DMFC) system that is suitable for use as a power supply for handheld electronic devices such as portable audio players and Bluetooth™ headsets for mobile phones.

Small fuel cells are drawing attention as a power supply for the support of the ubiquitous society, and the development of active type fuel cells is advancing for note PCs.

It is difficult to miniaturize the active-type DMFC, because a pump is required for feeding methanol, although the output of the conventional active-type is large.

In the passive-type fuel cell developed, miniaturization is facilitated by eliminating the pump and using high concentration methanol as a fuel by developing a new high power MEA (Membrane Electrode Assembly: the assembly of membrane and catalyst which generates electricity).

The size of the prototype DMFC is 22 mm×56 mm, which is about the size of a human thumb. It can operate a portable audio player continuously for 20 hours.

It was certified by Guinness as the smallest fuel cell in the world in February, 2005.

## 32-Class OCB-Mode Low Temperature Poly-Si TFT-LCD



32-class OCB-mode low temperature poly-Si TFT-LCD

Toshiba Matsushita Display Technology Co., Ltd. has developed a 32-class low-temperature polycrystalline silicon (hereinafter referred to as "poly-Si") (LTPS) thin-film transistor liquid crystal display (TFT-LCD) in which optically compensated bend (OCB) technology is applied.

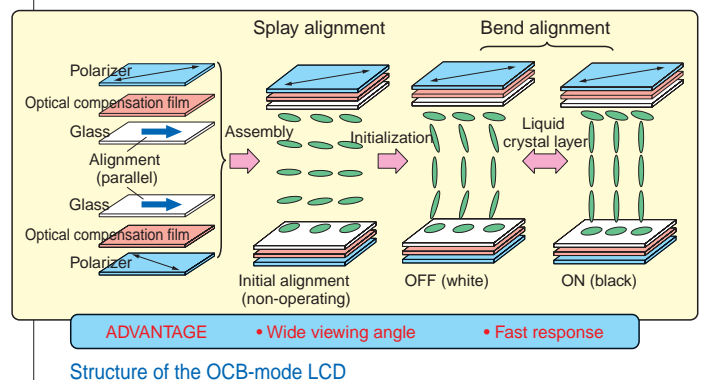
OCB technology can realize wide viewing angle and fast response characteristics, which are the weak points of current LCDs.

This time, we have improved response time by an order of magnitude (response time of 5 ms) compared with current LCDs, and have realized a quality of moving picture images in the newly developed LCD on a par with that on a cathode ray tube (CRT).

We started mass production of the 23-class OCB-mode TFT-LCD for television for the first time in the world in October, 2004.

Furthermore, we have succeeded in developing a 32-class OCB-mode LTPS TFT-LCD (1,366×768 pixels) as the world's largest size LTPS TFT-LCD.

In April 2005, we won the special prize of advanced display of the year (ADY) with OCB technology.



Structure of the OCB-mode LCD